Asian Journal of Convergence in Technology Volume III, Issue II
ISSN No.:2350-1146, I.F-2.71

Effective Low Power Testing strategy with respect to Built in Self-Test(BIST): A Survey

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Abstract
Low-power VLSI circuits are indispensable for modern electronic devices, and numerous hardware/software-based techniques have been developed for drastically reducing functional power dissipation. However, testing such low-power devices has increasingly become a severe challenge, especially in at-speed scan testing. The reason is that functional constraints with respect to circuit operations and clocking are mostly ignored in at-speed scan testing, which may result in test power that is 3X to 8X higher than functional power. This paper presents different low power techniques which can be applied to reducing the test power of Built in Self Test (BIST) circuits used for various digital IC's.

I.INTRODUCTION

The device density and the operating frequency were low enough in the past that power dissipation was not a constraining factor in VLSI chips. Nowadays, increased device density, speed and complexity have increased the power dissipation of the chip. The continuous demands from the user to expand the functionality of portable devices, without affecting the key product features, imposes tight constraints on the design technology with power optimization as its focal point .The amount of heat generated also limits the density of a chip. This power dissipated is contributed both by the actual power consumed by the circuit during normal operation and also by the test power. Test power is the power consumed by the circuit during testing. The dynamic power is mainly due to the switching activities of the circuit which may be attributed to the switching transient current and the charging and discharging of load capacitances during switching from one logic level to another level in the signal lines of the circuit. By reducing the dynamic power, majority of power saving can be obtained. As a result, lot of low power design techniques has been proposed at all levels of design hierarchy, with majority of these methods focusing on power dissipation in normal mode rather than in the test mode.

II LOW-POWER TEST

A high density system like ASIC or SoC always demands the nondestructive test which satisfies all the power constraints defined during design phase. On the other way, the current testing philosophy demands much more power consumption during test compared to power consumption during functional m ode. This section describes the reasons and effects of such high-power consumption.

A. Reasons of High-Power Consumption during Test.

There are several reasons for this increased test power. Out of them, the main reasons are as follows.
(i) The test efficiency has been shown to have a high correlation with the toggle rate; hence, in the test mode, the switching activity of all nodes is often several times higher than the activity during normal operations.
(ii) In an SoC, parallel testing is frequently employed to reduce the test application time, which may result in excessive energy and power dissipation.
(iii) The design-for-testability circuitry embedded in a circuit to reduce the test complexity is often idle during normal operations but may be intensively used in the test mode.
(iv) That successive functional input vectors applied to a given circuit during system mode have a significant correlation, while the correlation between consecutive test patterns can be very low. This can cause significantly larger switching activity and hence power dissipation in the circuit during test than that during its normal operation [3].

B. Effects of High-Power Dissipations.

The most adverse effect of very high-power dissipation during test is the destruction of IC itself. In addition, to prevent the IC from destruction, the power dissipation during test can affect the cost, reliability, autonomy, performance-verification, and yield-related issues [4]. Some of the effects are as

follows. (i) The growing need of at-speed testing can be constrained because of the high-power dissipation. So stuck at faults can be tested without any effect, but the testing of the delay fault will become difficult. (ii) During functional testing of the die just after wafer etching, the unpackaged bare die has very little provision for power or heat dissipation. This might be a problem for applications based on multichip module technology, for example, in which designers cannot realize the potential advantages in circuit density and performance without access to fully tested bare dies [5]. (iii) Circuit can be failed because of erosion of conductors caused by electro migration. (iv) The online BIST in battery-operated remotes and portable systems consumes very high power for testing only. Remote system operation occurs mostly in standby mode with almost no power consumption, interrupted by periodic self-tests. Hence, power savings during test mode directly prolong battery lifetime. (v) The elevated temperature and excessive current density severely decrease circuit reliability. (vi) Because of excessive power dissipation, the simple low-cost plastic packages used in consumer electronics cannot be used, but expensive packages which can remove the excessive heat are forced to be used.

III LOW POWER TECHNIQUES

A. Low-Power Test Pattern Generation

Test pattern generation is main part of testing circuits by which switching activity can be decreased. Power can be reduce during testing by low power test compaction, low power X-filling, and test vector ordering.[1] With the help of this technique two problems, like circuit overheat and performance degradation can be overcome.

B. Low power test compaction

The requirement of compaction is to reduce number of test vectors. Test cube can be exploited using test compaction, test cubes are the test vector containing unspecified bits or X- bits. Test data compaction can be done as dynamic compaction and static compaction. Dynamic compaction specifies the X-bits in a test cube in order to detect more faults than the initially targeted fault, while static compaction uses the X-bits in compatible test cubes to merge them into one test cube. [3]

	Compression ratio		
Benchmarks	Golomb	Huffman	Arithmetic
S5378	48%	50%	65%
S9234	57%	54%	66%
S13207	82%	69%	86%
S15850	65%	60%	75%
S35932	13%	55%	70%
S38417	45%	51.5%	70%
S38584	54%	53.5%	69%
Average	52%	56%	72%

Table 1 compression ratio

C Low power test ordering

There are many different techniques for test vector ordering which are as follow,

1.Artificial Intelligence Approach to Test Vector Reordering With the help of this technique we can overcome the problems like reliability and short term malfunction. In this technique, we have reduced dynamic power consumption during test application without losing stuck-at fault coverage. [5]

2. Scan chain reordering Using scan chain reordering the overall average power and peak power are reduced. In this method fault coverage, test application time, and hardware area overhead is negligible. [6]

3.Low-Power X-Filling As some of the test vectors are left with unspecified value; for example 10X01X. In X filling technique each X bit is replaced by 0 or 1. The main point is to reduce the number of transition in scan cell which leads to the reduction in overall switching.

- MT-Filling: 0001100111 (3 transitions)
- 0-Filling: 0001000100 (4 transitions)
- 1-Filling: 0111101111 (3 transitions)

IV LOW-POWER BIST TECHNIQUES

In the following, I categorize these techniques for low power BIST.

1.Test scheduling algorithms: This consists of a distributed BIST control scheme that simplifies the BIST execution of complex ICs, especially during higher test activity levels.3 This approach can schedule the execution of every BIST element to keep the power dissipation under specified limits. The technique reduces average power and consequently avoids temperature-related problems.

2. Low-power test pattern generators: This consists of a BIST strategy, called dual-speed LFSR, based on two different speed LFSRs. Its objective is to decrease the circuit's overall internal activity by connecting inputs that have elevated transition densities to the slow-speed LFSR. This strategy

significantly reduces average power and energy consumption without decreasing fault coverage.
3.Toggle suppression: This low power strategy is used for scan-based BIST architectures. This technique modifies the scan-path structure's scan cells in such a way that CUT Low-Power Testing 88 IEEE Design & Test of Computers inputs remain unchanged during a shift operation. This novel design for scan-path elements allows for energy savings that are from 70% to 90% of that for a standard, scan-based BIST architecture. At the same time, however, the technique increases the area overhead and may lead to performance degradation.

4. LFSR tuning : The problem of energy minimization during test application for BIST enabled circuits is analyzed here. The main constraint is reducing energy consumption without modifying the stuck-at fault coverage. In this work, the authors first analyze the impact of an LFSR's polynomial and seed selection on the circuit's switching activity during test application. They determine that the polynomial selection does not influence energy consumption; the LFSR's seed selection is a more important parameter. Therefore, the authors propose a method based on a simulated-annealing algorithm to select an LFSR's seed and provide the lowest energy consumption.

5. Vector filtering BIST: Here a test-vector-inhibiting technique is used to filter out some non detecting subsequences of a pseudorandom test set generated by an LFSR. The authors use a decoding logic to store the first and last vectors of the non detecting subsequences to be filtered. A D-type flip-flop, working in toggle mode, switches the enable/disable mode of the LFSR outputs to perform selective filtering.

6. Low power RAM testing : This strategy is based on RAM transition reduction by reordering the read and write accesses and the address counting scheme. These measures decrease the energy consumption and keep test time the same, so they also minimize the average power.

V RESULTS

The result shows power reduction done using different technique, this comparison is essential in order show the reduction in power during testing. We note that the average power consumption is greater but the difference between peak power is less.

Sr.No	Techniques	Approx. Power reduction
1	Low-Power Test Pattern	15% [1]
2	Low power test compaction	11% [3]
3	Low power test ordering	22% [4,6]
4	Low-Power X- Filling	5%[8]
5	Test Data Compression	9% [9]
6	Genetic Algorithm for VLSI Test vector Selection	10% [10]

VI CONCLUSIONS

IT'S NOT EASY to select an effective low-power testing strategy, given the number and the diversity of available techniques; the ultimate selection depends on several parameters. Obviously, the first parameter is the implementation context. Whether the technique is for external testing, scan, scan BIST, or parallel BIST, each context will lead to completely different choices. For example, test engineers can use a testvector-ordering technique during external or scan testing, but they cannot use it for pseudorandom BIST. The second parameter concerns the way DFT engineers want to address test power minimization. Do they want to act on the test sequence or on the test architecture? In the first case, DFT engineers select test-vector-ordering or compaction techniques (for external or scan testing). In the second case, DFT engineers prefer techniques like those presented May–June 2002 89 by Whetsel; Sankaralingam, Pouya, and Touba; and Bonhomme.28,31,32 A third parameter is the possibility that a designer or test engineer will have to relax some of the classical test constraints when implementing such a low-power testing technique. Actually, there are several relevant criteria to consider when selecting solutions for minimizing test power. Fault coverage and test time, among the main test constraints, must remain unaltered by the implemented technique.
So, although these techniques all minimize test power, each has a different effect on the various criteria. Consequently, each individual designer or test engineer will select a different low-power testing technique, depending on the importance attached to particular criteria for a given implementation.

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