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VLSI ARCHITECTURES FOR 2-D DISCRETE WAVELET TRANSFORM USING KS ADDER

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***Abstract*—Discrete wavelet transform (DWT) is a mathematical technique that provides a new method for signal processing. It decomposes a signal in the time domain by using dilated / contracted and translated versions of a single basis function. The 2-D DWT is highly computation intensive and many of its application need real-time processing to deliver better performance. The 2-D DWT is currently implemented in very large scale integration (VLSI) system to meet the space-time requirement of various real-time applications. Several design schemes have been suggested for efficient implementation of 2-D DWT in a VLSI system. The proposed 2-D DWT is implementation in Vedic multiplier with kogge stone adder. This design is efficient area and minimized delay in existing design.**

Keywords— Discrete Wavelet Transform, Vedic Multiplier, Kogge Stone Adder.

I. INTRODUCTION

The wavelet transform (WT) provides a time-frequency representation of the signal. It was developed to overcome the short coming of the short time Fourier transform (STFT), which can also be used to analyze non-stationary signals. While STFT gives a constant resolution at all frequencies, the WT uses multiresolution technique by which different frequencies are analyzed with different resolutions. The wavelet analysis is done similar to the STFT analysis. The signal to be analyzed is multiplied with a wavelet function just as it is multiplied with a window function in STFT, and then the transform is computed for each segment. A wavelet is a short oscillating function which contains both analysis function and the window function. In WT, time information is obtained by shifting the wavelet over the signal, while the frequencies are changed by contraction and dilatation of the wavelet function. The continuous wavelet transform (CWT) retrieves the time-frequency content information with an improved resolution compared to the STFT [Louis et al. (1997)].

Discrete wavelet transform (DWT) is a mathematical technique that provides a new method for signal processing and decomposes a discrete signal in the time domain by using dilated / contracted and translated versions of a single basis function, named as prototype wavelet [Mallat (1989a) ; Mallat (1989b) ; Daubachies (1992) ; Meyer (1993) ; Vetterli and Kovacevic (1995)]. DWT offers wide variety of useful features over other unitary transforms like discrete Fourier transforms (DFT), discrete cosine transform (DCT) and discrete sine transform (DST). Some of these features are; adaptive time-frequency windows, lower aliasing distortion for signal processing applications, efficient computational complexity and inherent scalability [Grzesczak et al. (1996)]. Due to these features one dimensional (1-D) DWT and two dimensional (2-D) DWT are applied in various application such as numerical analysis [Beylkin et al. (1992)], signal analysis [Akanshu and Haddad (1992)], image coding [Sodagar et al. (1999); Taubman (2000)], pattern recognition [Kronland et al. (1987)], statistics [Stoksik et al. (1994)] and biomedicine [Senhadji et al. (1994)]. Several algorithms and computation schemes have been suggested during last three decades for efficient hardware implementation of 1-D DWT and 2-D DWT.

II. Computation Scheme for DWT

In DWT, the info flag is decayed into two sub-groups known as low-pass sub-band and high-pass sub-band. The low-pass and high-pass sub-band segments of a specific DWT decay level is gotten by sifting the information flag utilizing a couple of low-pass and high-pass channel. The low-pass and high-pass channel match frames a quadrature reflect channel (QMF) for impeccable flag remaking. The low-pass and high-pass channels are short length limited motivation reaction (FIR) channel As shown in Figure 1, the low-pass filter output is down-sampled to obtained the low-pass sub-band output (ul(n)). Similarly, the high pass filter output is down-sampled to obtained the high-pass sub band output (uh(n)). The 1-D DWT computation is equivalent to a two channel down-sampled FIR filter computation. The filtering unit (FU) of 1-D DWT constitutes a pair of filters (low-pass filter (LPF) and high pass filter (HPF)), and a pair of down samplers.

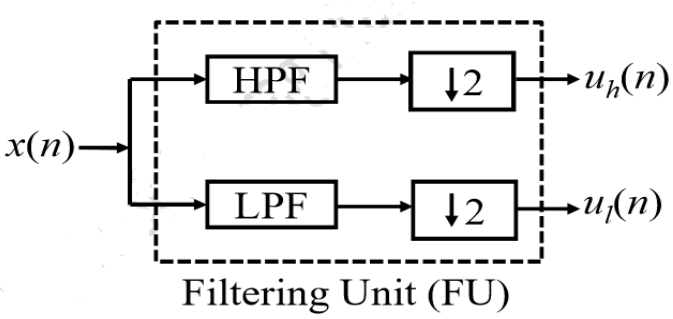


Figure 1: Computation of one level 1-D DWT

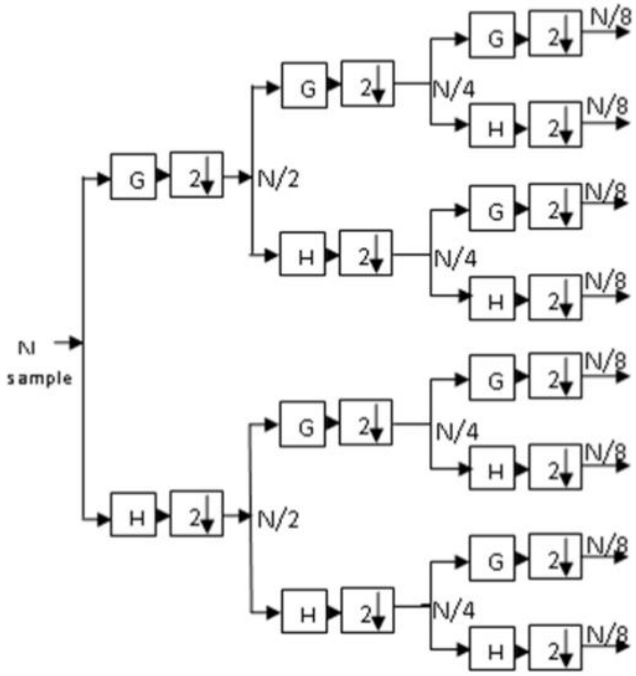


Figure 2: Complete 3-levels for 2-D DWT. G and H are the high-pass and low-pass filters respectively.

In Figure 2, assume that the first flag x[n] has 512 specimen focuses, spreading over a recurrence band of zero to π rad/s. At the principal deterioration level, the flag is gone through the high pass and low pass channels, trailed by subsampling by 2. The yield of the high-pass channel has 256 focuses (henceforth a fraction of the time determination), however it just traverses the frequencies π/2 to π rad/s (thus twofold the recurrence determination).

III. PROPOSED METHODOLOGY

In Figure 3, at the first decomposition level the original signal X[n] has N- sample points, is passed through 1×2 demultiplexer. When select line is 0 then we get even sample and when select line is 1 then we get odd sample. After that we have passed these samples through low-pass filter, same process with high-pass filter. Now we get N/2 samples at the first decomposition level output of multiplier based architecture for 2-D DWT is high-pass (Y_H) and low-pass filter (Y_L).

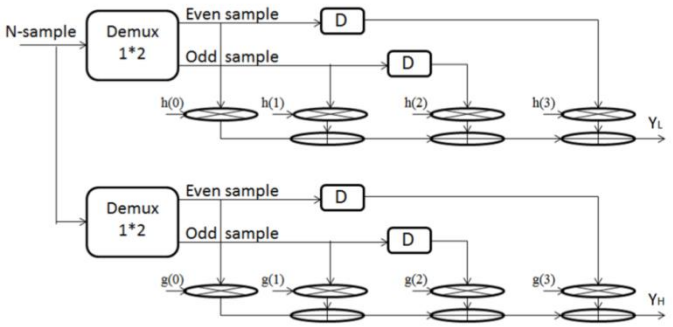


Figure 3: First decomposition level of multiplier based architecture for 2-D DWT including down sample by 2.

First level 2-D DWT consists of DE multiplexer, delay unit, multiplier and adder. Multiplier consumed more space compared to adder. So we are going to Kogge Stone (KS) adder based Vedic multiplier.

IV. Vedic Multiplier using KS Adder:-

Vedic multiplier and Kogge-Stone can compare with conventional method which is computed by Vedic multiplier, full adder and half adder. Proposed technique provides less path delay and less area. Input sequence of Conventional method is much more than to proposed method, however proposed method has less propagation delay. Territory and proliferation deferral can be lessened by the guide of adjusted KS snake. This viper will be planned like as swell convey snake. Convey yield of one KS viper is associated with another KS snake however this technique is exceptionally recipient for high effective computerized gadgets according to concerning proliferation delay.

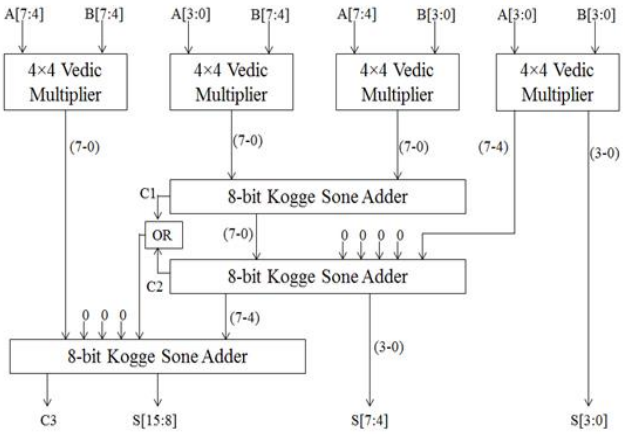


Figure 4: Logic Diagram of Vedic Multiplier using Kogge Stone Adder

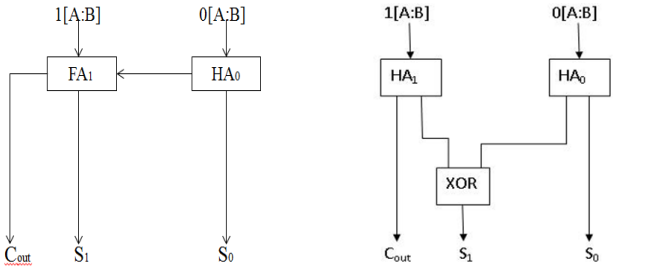
KS Adder:-
Inevitably, all the outlining levels of computerized framework or IC's Packages rely on upon number of entryways in a solitary chip that is likewise rung base approach. Adjusted KS viper can be decreased with respect to the range or number of entryways. In the event that we expel the primary XOR entryway from altered KS snake nothing will be changed for result yet zone and spread deferral will be diminished.

$$S_i = P_i \quad (1)$$

This condition is connected just for first summation yield. For the following entirety bit condition will be changed.

$$S_i = P_i \oplus G_{i-1} \quad (2)$$

In this proposed diagram excluded the first XOR gate. The sum bit of the first half adder shows the LSB bit of the output and carry output will connect to the first pin of XOR gate. The sum bit of the second half adder is connected to the second pin of the XOR gate. And the last carry output is the MSB bit of the output. Worked can be enhanced for the high bit information.



(a) (b)

Figure 5: (a) Previous Adder, (b) Proposed Adder

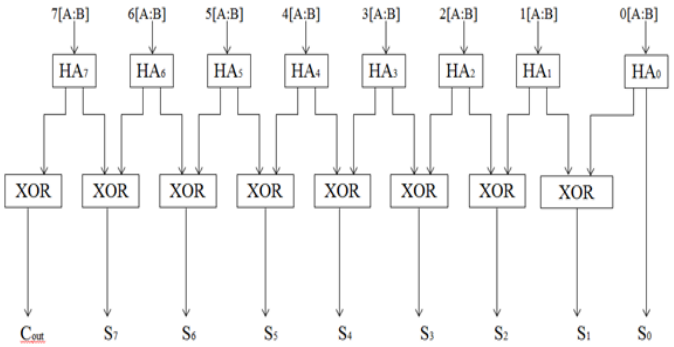


Figure 6: Proposed Diagram of 16-bit Kogge Stone Adder

Parameter Calculate:-

Number 4-input LUTs:- LUT stands for look up table that reduces the complex mathematics calculations and provide the reduced processing time. Look up table uses so many complex

applications such as signal processing, image processing, device modeling and other digital processing etc.

Number of Slices: - If the devices are connected in parallel form then it is called array of the devices. Generally look up table are comprised with number of slices. If the numbers of slices are increased then area will be increased. Numbers of slices are used less as possible as for better result and speed.

Propagation Delay:- Generally, the ideal condition of the result is the output of the digital circuit should from level 0 to level 1 or level 1 to level 0 in zero time. But in practice, it takes finite time to switch output levels. The time required to change output levels is called output switching time. It defines separately for switching from level 0 to level 1 and level 1 to level0.

Number of IOBs:- Input output buffers are related to the fan in and fan out of the circuit. Number of gates is dependent on numbers of IOBs. So, for low propagation delay IOBs must be less.

V. SIMULATION RESULT

We have implemented the proposed Vedic Multiplier using Kogge stone adder base on digital circuit. Basic architecture of Vedic multiplier Consists of full adder and half adder which requires less time to compute result. We have device summary of proposed multiplier and existing algorithm to achieve good computation speed compare to other shows in table 1 and table 2. Show the bar graph of the proposed design in figure 7 and figure 8 respectively.

Table 1: Comparisons Result for proposed design and existing algorithm

Design	Width	Area court
BEC Based Adder [2012]	8	188
	16	376
	32	752
CSLA Adder [2014]	8	133
	16	266
	32	532
Ms. G. R. Gokhale [2015]	8	104
	16	208
	32	416
Proposed Adder	8	83
	16	166

	32	332

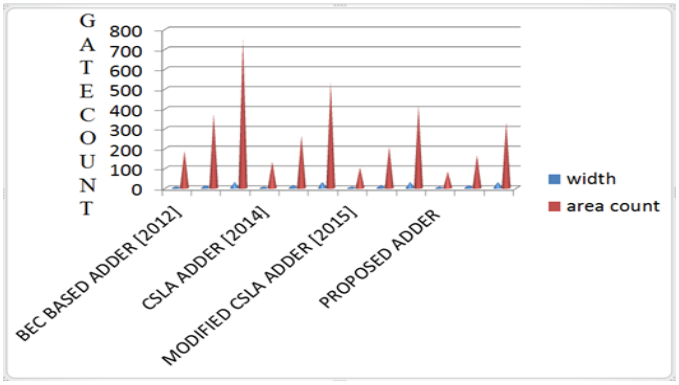


Figure 7: Bar Graph of the different types of adder

Table 2: Device utilization summary of 8-bit Vedic Multiplier

Design	*Width*	*Area count*	*MCPD*
P. Y. Bhavani [2014]	8-bit	1545	41.696 ns
G. Gokhale [2015]	8-bit	1380	45.678 ns
G. Gokhale [2015]	8-bit	1293	44.358 ns
Proposed Vedic Multiplier	8-bit	978	24.103 ns

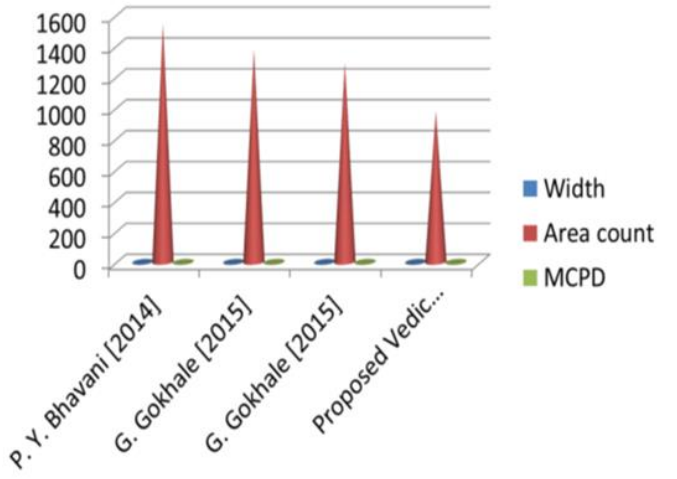


Figure 8: Bar Graph of the different Vedic Multiplier

Table 3: Device utilization summary of 2-D DWT

Design	*Width*	*Area count*	*MCPD*
Existing 2-D DWT	8-bit	17845	67.696 ns
Proposed 2-D DWT	8-bit	13353	52.542 ns

VI. CONCLUSION

The proposed parallel and folded architectures are individually best amongst the existing structures. These designs have specific features like throughput scalability, memory efficiency, higher memory utilization efficiency and regular data flow. These features are very useful for hardware implementation of 2-D DWT structure to meet area, speed and power requirement of different image processing applications. However, proposed structures have few shortcomings like critical path delay, fixed point error, and interconnect delay which could be further investigated to minimum the area-delay-power of the 2-D DWT structures. These issues will be addressed in the future work.

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