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Analysis and Comparison of Methods to Reduce Leakage Power and Latency to Improve Performance of VLSI Circuits

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***Abstract*: Power dissipation in one of the major concerns of VLSI circuit designers with the launch of battery held devices and applications, power consumption in the circuit also increased exponentially. Leakage current became an overriding factor in nanometer CMOS design technologies. This paper provides a comprehensive study, analysis and comparison of leakage power reduction technique such as zigzag approach, multi threshold approach, sleepy stack, dual sleep, transistor gating etc.. All the above methods are tested and analyzed using microwind EDA tool.**

Key Words*: *Leakage power, delay, multi threshold, sleepy stack ,dual sleep, transistor gating.

I. INTRODUCTION

Power consumption is an important issue in VLSI design. Today's focus is on low power devices because of growth in the mobile devices, but even before the introduction of mobile devices power dissipation was chronic issue. Higher power consumption leads to lower performance and reliability of the circuit. So number of methods proposed, introduced and implemented from device level to architectural level of CMOS circuit design, however complete reduction of power consumption is inevitable and no way to avoid tradeoff between power, area and latency are possible. There are only satisfying methods to reduce leakage power. As the technology trend took a new phase leakage power increased exponentially with more integration of transistors on a substrate. Leakage power is the static power which is dissipated when there is no useful outcome from the circuit or when circuit is idle. Whenever the gate voltage of transistor is lower than threshold voltage (V_{th}) transistor con not be completely turned off which leads to small current flow which is called as sub threshold current flow which is a leakage current. A report of International Technology Roadmap for Semiconductor indicates there might be a need of high valued dielectric material for low power and high performance. This paper gives a comprehensive study of satisfactory method to reduce leakage power in VLSI circuits.

II. LEAKAGE POWER

There are two kinds of power consumptions in the CMOS circuit. Dynamic power consumption which is inevitable to eliminate because of switching and computing activity where as static power consumption is leakage power which has prominent role in total power consumption. Static power dissipation is due to junction leakage – source to drain to substrate through reverse biased diodes, Gate induced drain leakage – high field effect in the drain of MOS transistor, Gate direct tunneling leakage – leakage through the oxide layers above the substrate which act as an insulator, Sub threshold leakage – current leakage of a transistor operating in weak inversion region. It is the largest leakage in CMOS circuit occurs because of lower threshold voltage in modern CMOS circuit.

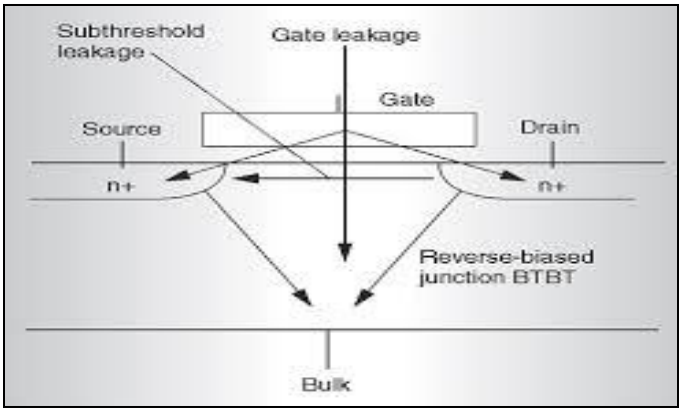

Fig 1. Leakages in CMOS circuit

III. LEAKAGE POWER REDUCTION TECHNIQUES

A. Sleep Approach

The most well-known traditional approach is the sleep approach. In the sleep approach, both (i) an additional "sleep "PMOS transistor is placed between VDD and the pull-up network of a circuit and (ii) an additional "sleep" NMOS transistor is placed between the pull-down network and GND. These sleep transistors turn off the circuit by cutting off the power rails. Fig. 2 shows its structure. A 2-input NAND gate with sleep transistors[1]. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively. However, output will be floating after sleep mode, so the technique results in destruction of state plus a floating output voltage.

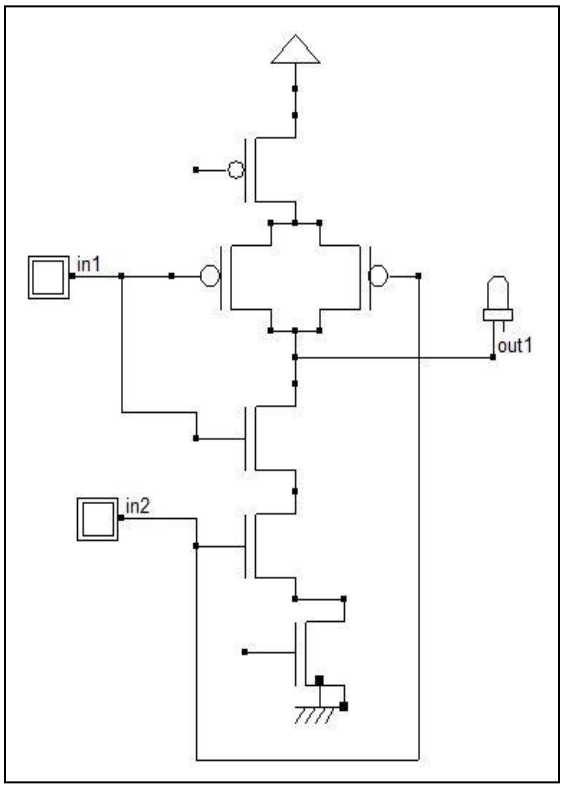

Fig 2. Sleep approach – 2 input NAND Gate

B. Zigzag Approach

The zigzag technique in Fig.3 uses one sleep transistor in each logic stage either in the pull-up or pull-down network according a particular input pattern. Input vector that can achieve the lowest possible leakage power consumption. Then, we either assign a sleep transistor to the pull-down network if the output is logic 1 or else assign a sleep transistor to the pull-up network if the output is logic 0. For Fig.3 we considered NAND-2 gate assuming that the output of the first stage is logic 1 and the output of the second stage is logic 0 when minimum leakage inputs are asserted. Therefore, we apply a pull-down sleep transistor for the first stage and a pull-up sleep transistor for the second stage. To reduce the wake-up cost of the sleep transistor technique, the zigzag technique is introduced.[6]

C. Sleepy Stack

In this technique it forces a stack effect by braking down existing transistor into 2 half size transistors.

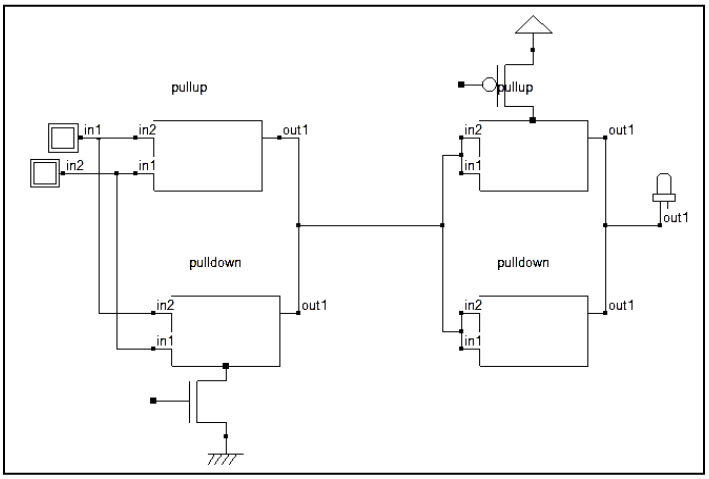

Fig 3. Zigzag approach

Fig.4 shows its structure. When the two transistors are turned off together, induced reverse bias between the two transistors results in sub threshold leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach. The sleepy stack approach combines the sleep and stack approaches. Between the divide transistors one of sleep transistor will be added in parallel. Stacked transistors suppress leakage current while saving state & Sleep transistors are turned off during sleep mode. In active mode it reduces delay & resistance of the path because of sleep transistor, sleep transistor is placed in parallel to the one of stack transistor.

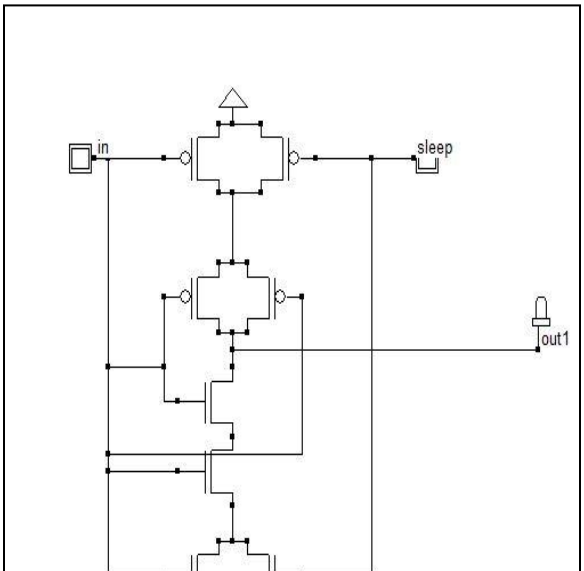

Fig 4. Sleepy Stack

D. Dual Sleep

Dual sleep Technique uses the advantage of using the two extra pull - up & pull-down transistors in sleep mode either in OFF/ON state. To all logic circuitry the dual sleep portion is designed as common [12]. For a certain logic circuit less number of transistors are enough to apply. The method is dual stack approach. Dual sleep approach is as shown in fig. 5 [7] [8]

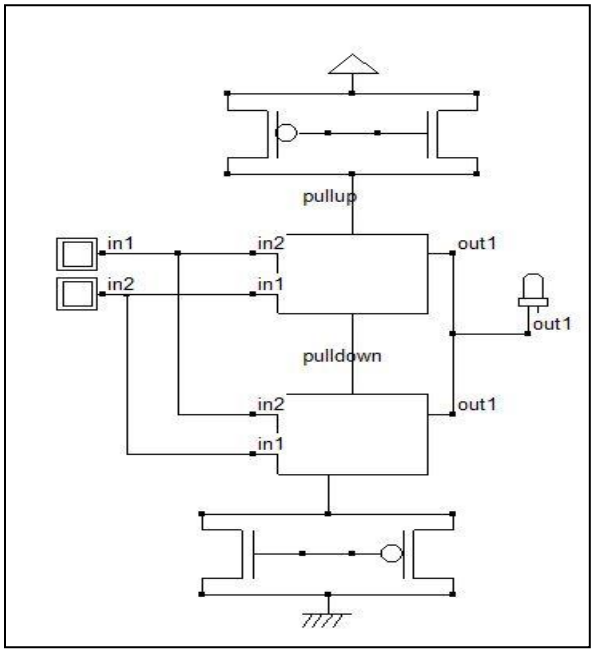

Fig 5. Dual sleep approach

As we can see in the fig.5 dual sleep uses set of NMOS and PMOS at both pull-up pull-down network. This has an advantage that NMOS degrades logic high and PMOS degrades logic low. Due to body effect further low in the voltage level hence pass transistor reduces voltage applied to the main circuit.

E. Sleepy Pass Gate

Sleepy pass gate which pass both 0 and 1. When the sleep signal on gate terminal of PMOS is a Logic 0, then its complement sleep bar (Logic 1) is applied to gate terminal of NMOS, allowing both transistors to conduct and pass the signal at IN to OUT. When the sleep signal on gate terminal of PMOS is a Logic 1, complementary Logic 0 is applied to NMOS gate, turning both transistors off and forcing a high-impedance condition on both IN and OUT nodes.[8] This high-impedance condition represents third "state" (high, low, or high-Z). Thus, pass gate acts as an open circuit offering high impedance. This design acts as a voltage controlled resistor connecting input and output providing true bidirectional connectivity without degradation of the input signal. Sleepy pass gate as shown in fig. 6

F. Sleepy Keeper

It is well known that PMOS transistors are not efficient at passing GND; similarly, it is well known that NMOS transistors are not efficient at passing VDD. However, to maintain a value of'1' in sleep mode, given that the '1' value has already been calculated, the sleepy keeper approach uses this output value of '1' and an NMOS transistor connected to VDD to maintain output value equal to '1' when in sleep mode[7]. As shown in fig.7, an additional single NMOS transistor placed in parallel to the pull-up sleep transistor connects VDD to the pull-up network. When in sleep mode, this NMOS transistor is the only source of VDD to the pull-up network since the sleep transistor is off.

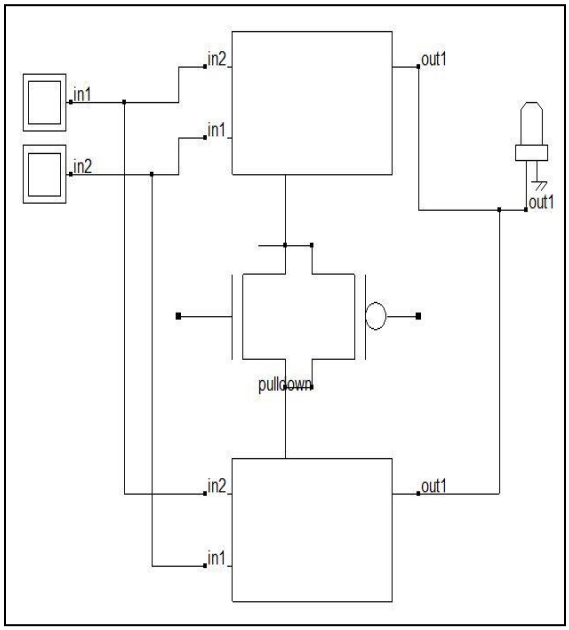

Fig 6. Sleepy pass gate

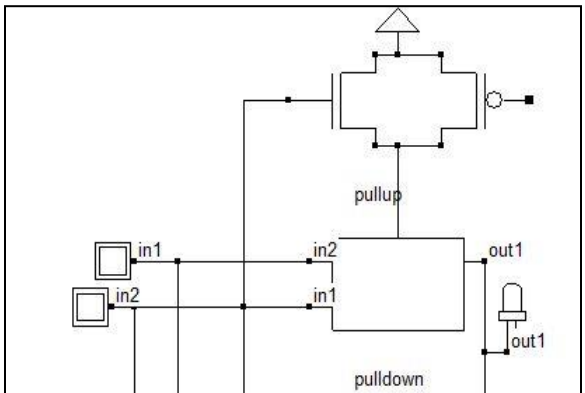

Fig 7. Sleepy Keeper

IV. ANALYSIS AND RESULTS

In this section we represent models simulated using microwind tool with 1.2µm technology. All the models have been given a power supply VDD of 5V (DC). Following fig. is a schematic of zigzag method implemented using microwind.

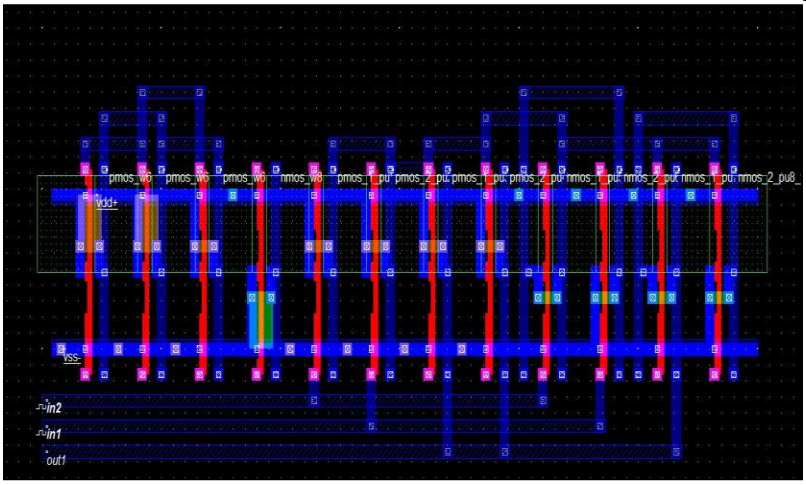

Fig.8 Zigzag approach schematic

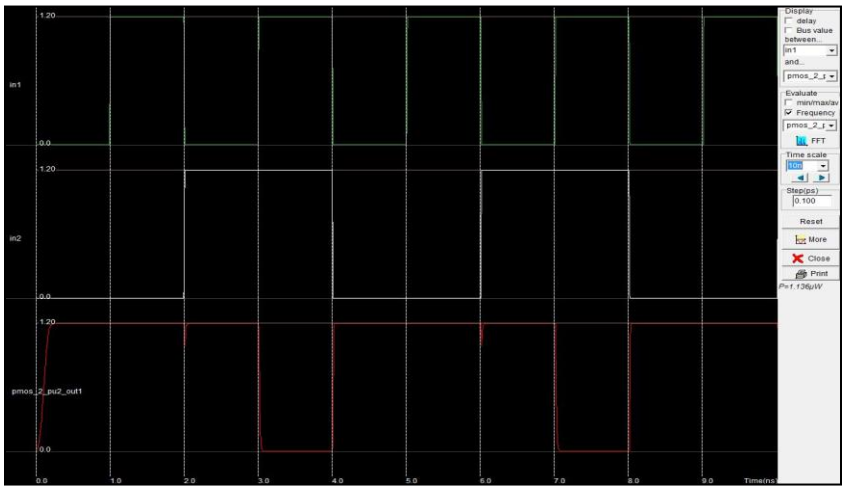

Fig 9. Voltage v/s Time characteristic of zigzag approach

If we closely observer Fig 9 the timing diagram red in color is output of NAND 2 gate. By using Voltage v/s Current characteristic graph power consumed is calculated shown as below.

Table1.Leakage power of different approaches

Technique	Leakage Power(µW)
Sleep approach	0.040
Zigzag approach	0.038
Sleepy Stack	0.05806
Dual Sleep	0.0347
Sleepy keeper	0.085
Sleepy Pass Gate	0.0287

From the table the best suitable method can be used is sleepy pass gate, though it consumes less power area required to implement it is more which can be analysed from following fig 10.

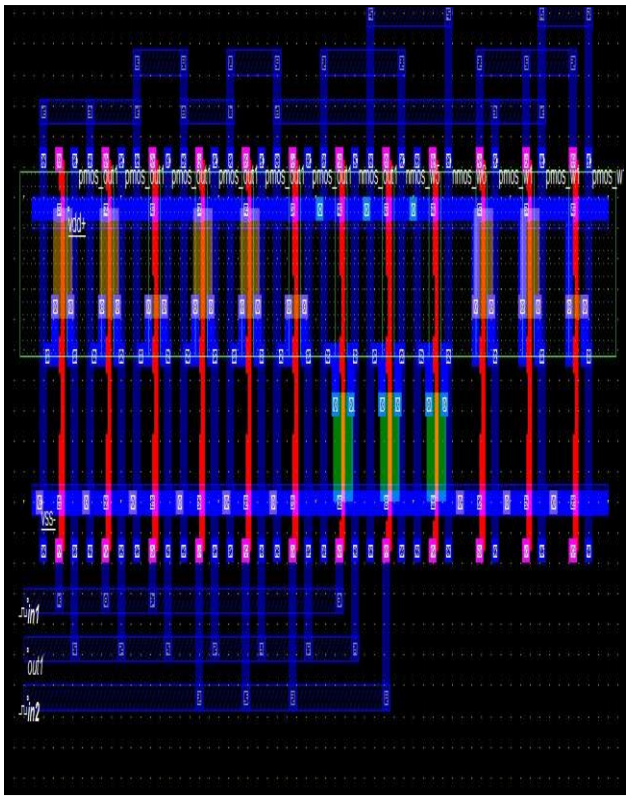

Fig10. Sleepy pass gate approach

It can be clearly visualized out of fig.8 and fig.10 the more area consumed is by sleepy pass gate method. There exists tradeoff between area and power consumption which is inevitable. Area required to implement NAND2 gate according to microwind tool using 1.2µm technology is as follows.

Table2. Area required for implementing NAND 2 g gate

The following graph helps to analyze both area and power togrther and informs us how sleepy pass gate method distinguishes itself from other methods.

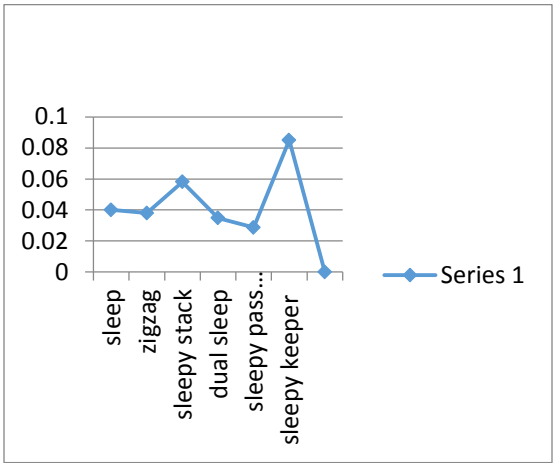

Fig11. Techniques v/s power consumption (µw)

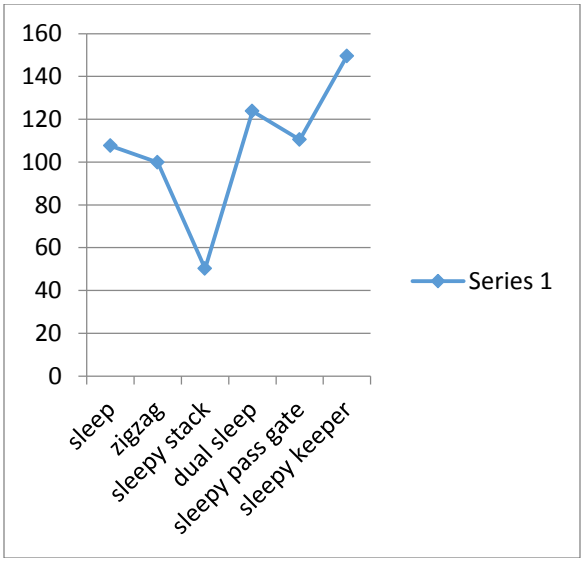

Fig12. Techniques v/s area required (μm^2)

V. CONCLUSION

In CMOS manometer technology leakage power dominates all other kinds of power dissipation hence it becomes major concern for VLSI designers thus introducing several techniques to reduce leakage power. This paper analyzed several methods used to reduce power and depicted always there is a tradeoff between power consumption and area required to implement the method so compromise has to be made while implementing.

Technique	Area in μm^2
Sleep approach	107.6
Zigzag approach	99.84
Sleepy Stack	50.22
Dual Sleep	123.76
Sleepy keeper	149.5
Sleepy Pass Gate	110.48

VI. REFERENCES

[1] M D Kamaruzzman, Soumithra Kumar Mandal "A Novel approach for leakage power reduction techniques in CMOS VLSI circuits" Proceeding of 12th IRF conference 26 June 2016 Hyderabad India
ISBN 978-93-86083-47-0

[2] Vinay Kumar Madasu, B Kedarnath "Leakage Power reduction using sleep method" "International Journal of Engineering and Computer Science ISSN 2319-7242 Volume 2 Issue 9 September 2013.

[3] Vikas Singhai, Saima Auybb, Paresh Rawath "Comparision of leakage power techniques in 65nm technology" International Journal of Computer applications (0975-8887) Volume 134 No 8, January 2016

[4]K Sailaja, V Leela Rani, SK Mahammad Akram "Analysis of Leakage power reduction technique for low power VLSI design" International Journal of Computer Applications(0975-8887) Volume 82 No 18, November 2013

[5] Shiro Kamohara, Nobuyuki Sugii, Yoshiki Yamamoto, Hideki Makiyama, Tomohiro Yamashita, Takumi Hasegaw, Shinobu Okanishi, Hiroshi Yanagita, Masaru Kadoshima, Keiichi Maekawa, Hitoshi Mitani, Yasushi Yamagata, Hidekazu Odal, Yasuo Yamaguchi1, Koichiro Ishibashi, Hideharu Amano, Kimiyoshi Usami, Kazutoshi Kobayashi, Tomoko Mizutani, Toshiro Hiramoto "Ultralow-Voltage Design and Technology of Silicon-on-Thin-Buried-Oxide (SOTB) CMOS for Highly Energy Efficient Electronics in IoT Era"

[6]Kausha Kumar Nigam, Ashok Tiwari "Zigzag Keeper a New Approach for Low Power CMOS circuit" International Journal of Advance Research in Computer and Communication Engineering Volume 1, Issue 9 2012

[7]Volkan Kursun, E G Friedman https://www.researchgate.net/publication/3337499_Sleep_switch_dual_threshold_Voltage_domino_logic_with_reduced_standby_leakage_current?enrichId=rgreq-5a291c86-9441-4a18-84a7-1462a723a04d&enrichSource=Y292ZXJQYWdlOzMzMzc0OTk7QVM6OTg5MTI2NjQ4MTc2NzdAMTQwMDU5NDAyNjAxMw%3D%3D&el=1_x_3

[8]Raju Hebbale, Pallavi Hiremath "Leakage Power reduction technique for Low Power VLSI design: A review Paper"

International Journal of Advance Research in Science and Engineering Volume No2 Issue 12, December 2013
[9] K. Gnana Deepika, K. Mariya Priyadarshini and K. David Solomon Raj "Sleepy Keeper Approach for Power Performance Tuning in VLSI Desig" International Journal of Electronics and Communication Engineering. ISSN 0974-2166 Volume 6, Number 1 (2013), pp. 17-28
[10]Se Hum Kim Vincent J Mooney3 Sleepy Keeper: a New Approach to Low-leakage Power VLSI Design
[11]Chu, R.C., Simons, R.E., and Chrysler, G.M., "Experimental Investigation of an Enhanced Thermo syphon Heat Loop for Cooling of a High Performance Electronics Module," Proceedings of the 15th IEEE Semiconductor Thermal Measurement and Management Symposium
[12] S.Samanta" Power Efficient VLSI Inverter Design using Adiabatic Logic and Estimation of Power dissipation using VLSIEDA Tool" Special issue of International Journal of computer communication Technology.vol 2.isuue 2,3,4.pp300-303. 2010.