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Design of OFDM MIMO Transreciever Model With Fast Fourier Transform in SIMULINK

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Abstract: The Orthogonal Frequency Division Multiplexing (OFDM) having multicarrier transmission. OFDM is useful in Frequency Selective Fading to reduce robustness. It having N number of non-overlapping sub channels. By combining of Multiple Input Multiple Output that is MIMO OFDM Transmit high data at a time to increase Data rate. [9]For OFDM MIMO transceiver operation FFT and IFFT is used. Using different parameters like Constellation , Convolutional code rate and the MIMO Parsing method transceiver operation is done.16 QAM at ½ code rate for 48 Mbps data rate with Spatial multiplexing. FPGA is used for Hardware Co-simulation.

Keywords: OFDM,MIMO,FPGA,QAM

I. INTRODUCTION

OFDM is a parallel transmission scheme, where a high-rate serial data stream is split up into a set of low-rate sub streams, each of which is modulated on a separates (FDM). Thereby, the bandwidth of the SCs becomes small compared with the coherence bandwidth of the channel; that is, the individual SCs experience flat fading, which allows for simple equalization. This implies that the symbol period of the sub streams is made long compared to the delay spread of the time-dispersive radio channel. By selecting a special set of (orthogonal) carrier frequencies, high spectral efficiency is obtained because the spectra of the SCs overlap, while mutual influence among the SCs can be avoided [2].

OFDM is a combination of modulation and multiplexing .OFDM is a method of encoding digital data on multiple carrier frequencies .OFDM helps in reducing intersymbol interference even at high data rate .MIMO stands for multiple input and multiple output .In this technology multiple antennas are used at both the transmitter and receiver to improve communication performance.

MIMO technology offers significant increases in data throughput and link range without additional bandwidth or increased transmit power .OFDM technique carried out in the digital domain, there are different methods to implemented the system .One of these Application Specific Integrated Circuit (ASIC) is being used.

The advantage of ASIC is it has fastest, smallest and lower power way to implement OFDM into hardware. Another method that can be used to implement OFDM is general purpose Microprocessor or Micro Controller. Field-Programmable Gate Array (FPGA) is an example of VLSI circuit[8]. This hardware is programmable and the designer has full control over the actual design implementation without the need (and delay) for any physical IC fabrication facility [5]. An FPGA combines the speed, power, and density attributes of an ASIC with the programmability of a general purpose processor will give advantages to the OFDM system. An FPGA could be reprogrammed for new functions by a base station to meet future needs particularly when new design is going to fabricate into chip. This will be the best choice for OFDM implementation since it gives flexibility to the program design besides the low cost hardware component compared to others.

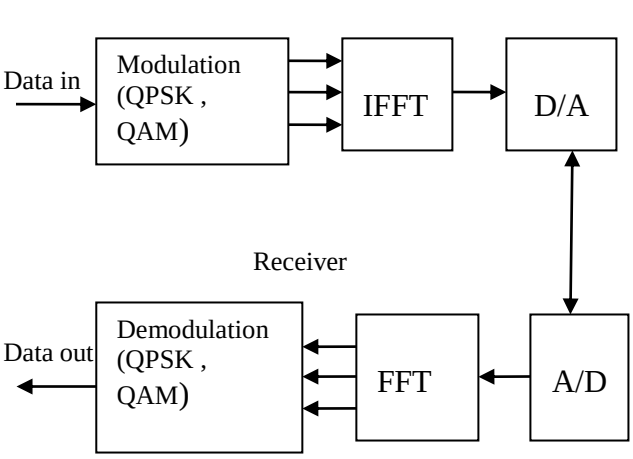

Fig.1.1: OFDM Transmitter and Receiver.

In this technique, the given bandwidth is shared among individual modulated data sources. Normal

modulation techniques like AM, PM, FM, BPSK, QPSK, etc... are single carrier modulation techniques, in which the incoming information is modulated over a single carrier [1].OFDM is a multicarrier modulation technique, which employs several carriers, within the allocated bandwidth, to convey the information from source to destination. Each carrier may employ one of the several available digital modulation techniques like BPSK, QPSK, and QAM.

A communications data stream is effectively split into N parallel low bandwidth modulated data streams. Each sub-carrier overlaps, but they are all orthogonal to each other, such that they do not interfere with one another. Each of the sub-carriers has a low symbol rate. But the combination of sub-carriers carrying information in parallel allows for high data rates. The other advantage of a low symbol rate is that inter-symbol interference (ISI) can be reduced dramatically since the symbol time represents a very small proportion of the typical multipath delay [1].

The transmitter stage of an OFDM transceiver takes data, converts, and encodes it into a serial stream before modulation. The OFDM signal is generated using an Inverse Fast Fourier Transform (IFFT). The receiver stage of the transceiver simply reverses the process.[7]

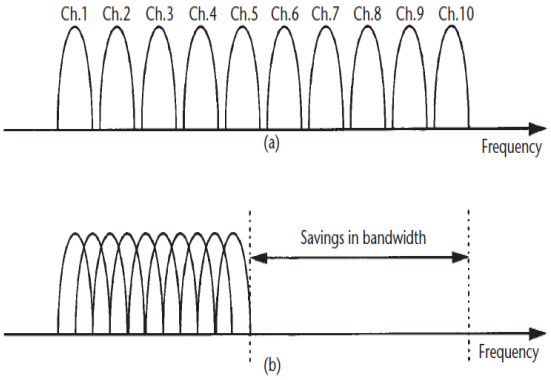

Fig.1.2: (a) conventional multicarrier technique, and (b) orthogonal multicarrier modulation technique.

I. SOFTWARE MODEL IMPLEMENTATION

The figure 2.1 represents the 4 x 4 MIMO model. 4 x 4 means there are four transmitters and four receivers. A real time audio signal is provided as input by connecting the Gateway In to the workspace with the help of a manual switch. The Gateway In block is required to convert input which is of Simulink type to Xilinx type. The input sampled voice signal is then fed to the parallel to serial convertor and then is applied to the Subsystem. [1]

The subsystem is the transmitter module while subsystem 1 is the receiver module.[3]The Gateways are used to convert Xilinx type to Simulink type output or vice versa. At the end a scope is connected where the first plot is for output of 4 x 4 MIMO model whereas the second plot is just the input signal applied to the model. The use of this is to verify whether the same signal is reproduced at the receiver side. A SNR of 15 dB is added in one of the channel to see the behavior. Displays, scopes are connected to get the readings and observe the signals at different points to get more clear idea of functioning of the entire system [4]

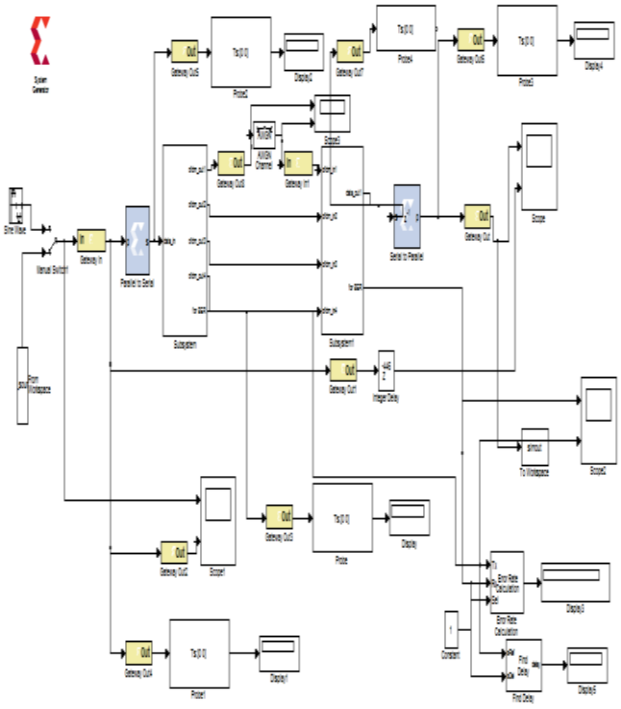

Fig.2.1: 4 x 4 MIMO model

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In order to observe the output of serial to parallel convertor block and actual input they are applied as third and fourth input to the scope respectively. The Gateway Out is used to convert the Xilinx type inputs to the Simulink type outputs.

II. THE TRANSMITTER SUBSYSTEM

It contains Encoder, Mapper, MIMO Parser, stream of OFDM.

3.1ENCODER:

The figure 3.10 shows the encoder module where there are two shift registers and two X-OR gates. Initially the shift registers have a zero bit stored in it. For the first X-OR gate there are three inputs.

The first input is as it is the output of parallel to serial block. The second input is output of parallel to serial block with one delay while the third is the output of parallel to serial block with two delays. The output of the first X-OR is given out as data out 1.

For the second X-OR gate there are two inputs. Both the inputs are outputs of parallel to serial blocks with one and two delays respectively. The output of the second X-OR is given out as data_out 2.

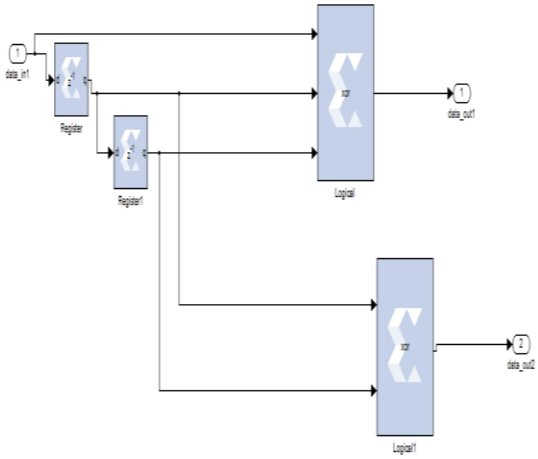


Fig. 3.1: Encoder Model

2.2 ENCODING TRUNCATING AND CONCATING :

In figure 3.2 the two outputs of encoder are truncated in the convert block separately and then are concated in the concat block. The concated output is fed to parallel to serial block and output of it is connected to the output port data out.

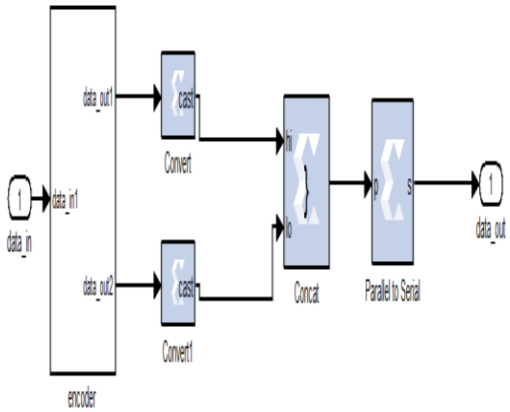


Fig 3.2: Encoder/Interleaver module

2.3 MAPPER:

The output of encoder/interleave module is applied as input to the Mapper. The combination of ROM_Imag, ROM_Real altogether forms QAM mapper. The ROM_Imag provides the value on imaginary axis while ROM_Real provides the value on real axis. This is giving up the points on different quadrants

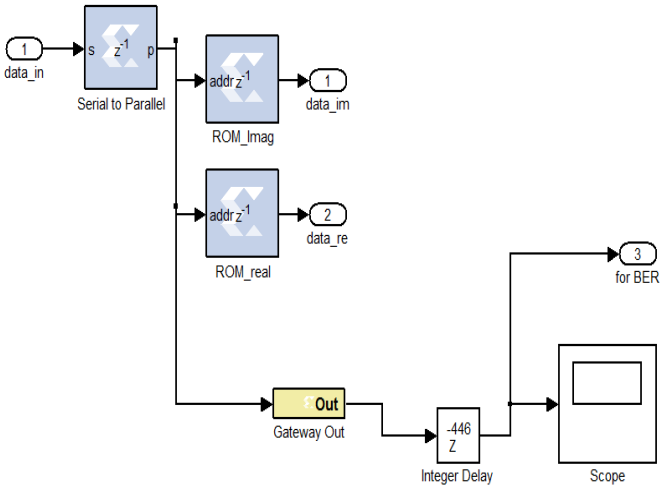


Fig. 3.3: Mapper

3.4 MIMO PARSER:

The ROM- Image and ROM Real are fed to the MIMO parser as In 1 and In 2 respectively. The main purpose of using a MIMO parser is to split the single stream input into two streams.

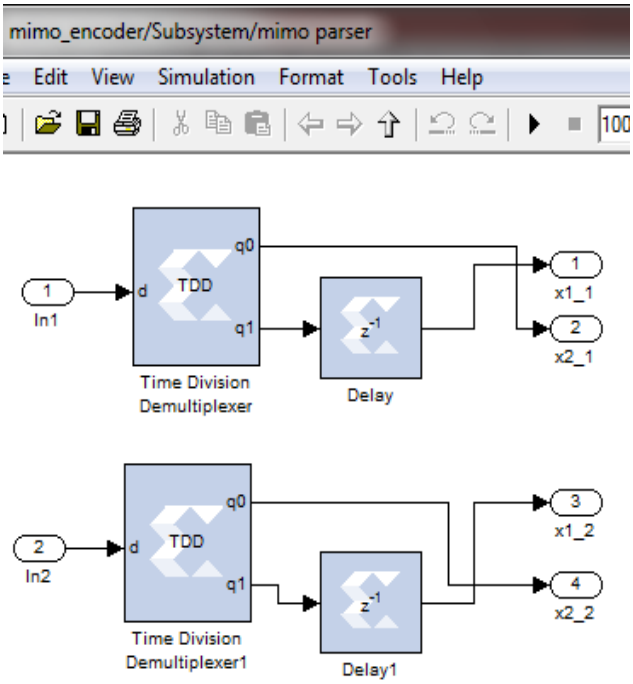
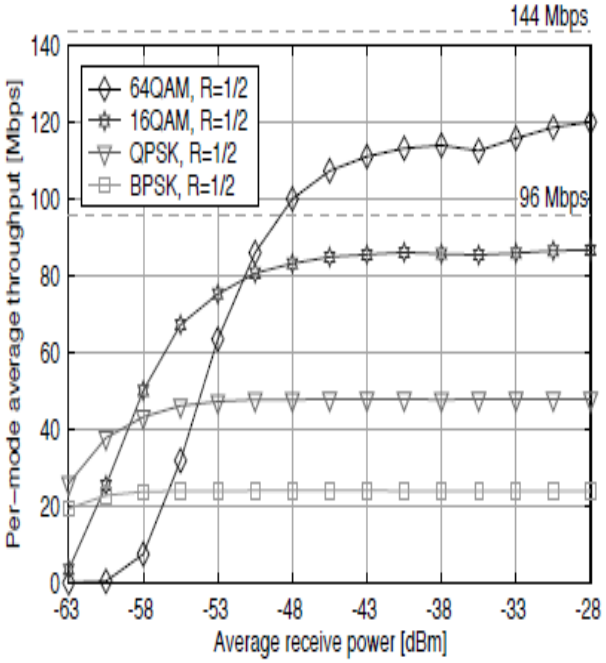


Fig. 3.4: MIMO Parser

As shown in figure 3.4 the MIMO parser is nothing but the combination of two Time Division



Demultiplexer (TDD) and two delay blocks. In TDD the sampled input is presented as two channels at the output. The ROM_Imag is splitted into two streams using TDD and a delay which is represented as x1_1 and x2_1. The ROM_Real is splitted into two streams represented as x1_1 and x2_2 using a TDD and a delay.

The output of mimo parser is connected to mimo parser 1 and mimo parser 2 so that 2 channels can be converted to 4 channels.

3.5 STREAM 1 (OFDM TX)

The first ROM Image and first ROM_Real i.e. the first and third outputs of MIMO parser1 (x1_1 and x2_2) are applied as inputs (In 1 and In 2) to the ofdm 1 block. Inside OFDM 1 block i.e. figure 3.5 we have the 64 size IFFT. The pilot and guard interval subcarriers are automatically inserted by this Xilinx block and the output is given at OFDM out 1.

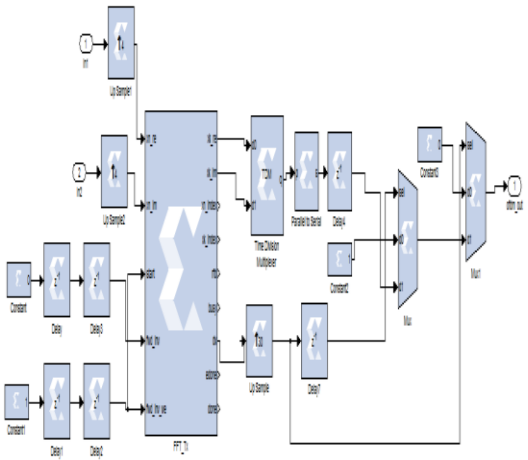


Fig. 3.5: OFDM TX

IV THE MIMO RECEIVER SUBSYSTEM

4.1 OFDM RX:

In OFDM RX FFT performs the exact reverse operation as that of the IFFT. It will remove the pilot and guard subcarriers and extract the ROM_Imag and ROM_Real i.e. x1_1 and x1_2 which are given at Out1 and Out 2 respectively.

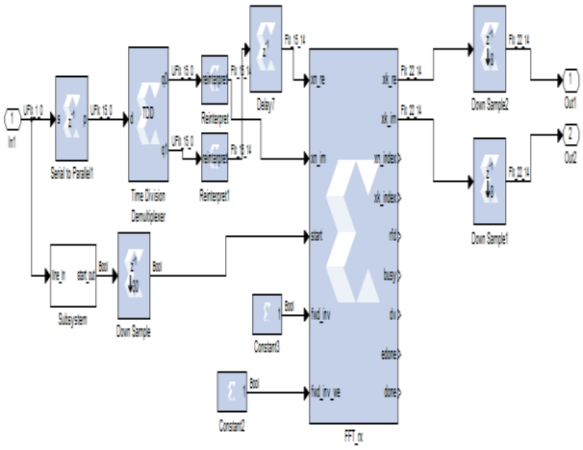


Fig. 4.1: OFDM RX

4.2 DECODER

The figure 4.2 represents the decoder which consists of serial to parallel block and a decoder block. A MATLAB code is written for the purpose of decoding the actual data.

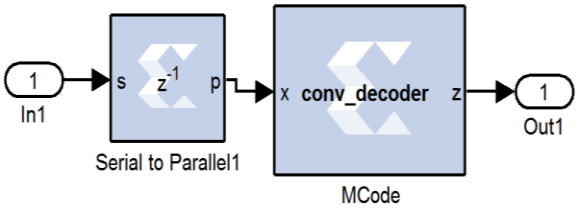


Fig 4.2: Decoder module

V RESULT

FPGA is superior method for implementation of OFDM compared to ASIC and Microprocessors. FPGA hardware is programmable and the designer has full control over the actual design implementation without the need (and delay) for any physical IC fabrication facility.

Fig 5.1: Actual Constellation Performance [7]

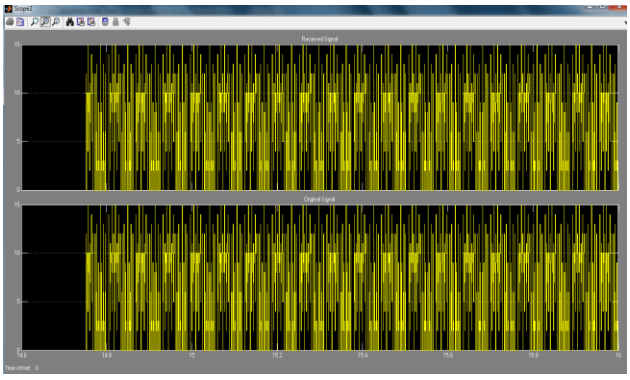


Fig. 5.2: Hardware co-simulation

VI.CONCLUSION

OFDM systems are the answer to our ever increasing data rate needs. By implementing a MIMO OFDM baseband transceiver on an FPGA by proper selection of one of the sixteen configurations we expect to fulfill the need for high-speed data transmission for a wireless communication system with reasonable prices of hardware implementation. We understand the challenges and opportunities available in the technology. Also the implementation on FPGA better than on a general purpose MPU in terms of speed and on ASIC in terms on cost. Also the FPGA can be easily reconfigured by the base station to meet future needs.

The successful implementation of the transceiver on a FPGA would pave a way towards developing 802.11n modem. The architecture is applied for realization of 802.16 (Wi-max) and LTE transceivers. It intends to study various alternatives for implementation of the OFDM which results in reduced chip size which by extension means cost reduction. Finally to develop a complete system of indigenously developed 802.11n modem which then results in robust, maximum throughput, highly scalable wireless LAN network.

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