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A HYBRID DSTATCOM TOPOLOGY FOR LOAD COMPENSATION WITH REDUCED DC-LINK VOLTAGE RATING

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***Abstract*— The Distribution Static Compensator (DSTATCOM) is mainly used for compensation of load in low voltage distribution system. The study proposes a Hybrid DSTATCOM topology that consists of a three-leg VSI with neutral clamped split capacitor to compensate unbalanced and non-linear loads. The scheme is employed with a series capacitor along with the interfacing inductance and a shunt capacitor. This reduces the required DC-link voltage and consequently reduces the voltage stresses on DC-link capacitor, while the shunt capacitor absorbs switching frequency harmonic components on supply side. The reference currents for the proposed hybrid DSTATCOM have been derived by using Synchronous Reference Frame Theory. The performance of proposed topology is verified using MATLAB/ SIMULINK.**

Keywords—Non-stiff source; DSTATCOM, Reduced DC-Link Voltage; Synchronous Reference Frame Theory (SRFT); Load compensation.

INTRODUCTION

Due to increased use of power electronic devices which comprise of non-linear loads and unbalanced loads the power quality in electrical distribution network has degraded [1], [2]. There are many ways to improve the power quality (PQ) [3]-[5].A distribution level static compensator is a newly developed STATCOM used in electric power distribution systems for power quality improvement [6]-[8].

The DSTATCOM is a shunt active filter that mitigates PQ problems by injecting current at point of common coupling (PCC). In practice, the load is remote from a distribution substation and in such cases load is supplied by the feeder impedance. The presence of feeder impedance causes distortion of source currents and PCC voltages due to inverter switching and this source is referred as a non-stiff source [9]-[11].

The performance of a DSTATCOM depends upon control algorithm used to extract the reference currents. In [12] various control algorithms are reported to demonstrate the behavior of DSTACOM. The compensation performance of DSTATCOM is studied for different faults and increasing load conditions. It is observed that the capacity for power compensation of DSTATCOM depends upon the voltage rating of DC-link capacitor [13], [14]. It has also been stated that the response of DSTATCOM is fast for compensation of the reactive power control devices [15]. In general, the DSTACOMs are operated at a fixed DC-link voltage value. When the DC-link voltage is less than the fixed value, there is insufficient resultant voltage to get the currents through inductors for reference current tracking and when DC-link voltage is higher than the limit, Voltage Source Inverter (VSI) becomes bulky and the switches employed in VSI must be rated for higher value of voltage and current. This results in an increased cost and size of VSI. So, the approach is to reduce DC-link voltage storage capacity.

In this paper, a three-phase, four-wire distribution system employed with a hybrid DSTATCOM topologyhas been proposed for load compensation which uses three legged VSI and two capacitors. Of these two capacitors, one is connected in series with the interfacing inductance and the other is in shunt with the active filter. The split capacitor neutral clamped arrangement is providedin which a neutral is connected between the two capacitors. The main contribution of the paper is that reference currents are generated using synchronous reference frame theory (SRFT) for the proposed topology. The performance of proposed topology and its control method is verified through simulation by using MATLAB / SIMULINK.

This paper is organized as follows. An overview of the proposed topology is presented in Section II. Section III focuses on the design of VSI and selection of its parameters. Control strategy for DSTATCOM is described in Section IV. Section V contains the simulation and its results while Section VI concludes this paper.

PROPOSED DSTATCOM TOPOLOGY

This section describes the power circuit diagram of three-phase proposed DSTATCOM topology applied in low voltage distribution network which is shown in Fig.1. It consists of a three-phase, four-wire, neutral clamped VSI and requires two DC storage capacitors [16]. In this figure, V_a, $V_b$and V_c are the source voltages of the phases *a*, *b* and *c* respectively. Similarly, I_a, $I_b$and I_c are the source currents of the phases *a*, *b*

and *c* respectively. The feeder impedance is composed of inductance L_s and resistance R_s in each phase of the system. V_{ta}, V_{tb} and V_{tc} are the terminal voltages and I_{la}, I_{lb} and I_{lc} are the load currents in the phases *a*, *b* and *c* respectively. The current in the neutral leg is represented as I_o. The loads consist of both linear and non-linear elements which may be balanced or imbalanced. The interfacing inductance and resistance are termed as L_f and R_f, respectively. The DC-link capacitors are represented by $C_{dc1}=C_{dc2}=C_{dc}$, whereas voltages maintained across the capacitors are $V_{dc1}=V_{dc2}=V_{dc}$.

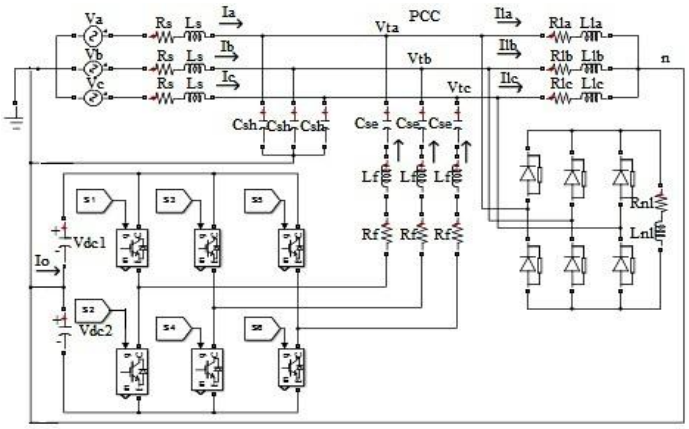


Fig.1: Schematic diagram of Proposed DSTATCOM topology

A capacitor C_{se} is integrated in series with the interfacing shunt branch of the active filter and a capacitor C_{sh} in shunt with the active filter. This proposed topology is also termed as a hybrid topology. The introduction of capacitor C_{se} with the interfacing inductance will reduce the DC-link voltage requirement and consequently reduces the average switching frequency of the switches. The shunt capacitance C_{sh} helps to eliminate the switching frequency component of VSI in terminal voltages and source currents using state feedback control. For the better performance of the DSTATCOM, the capacitors C_{se} and C_{sh} are designed carefully. The design procedure is explained in next section.

VSI PARAMETER DESIGN FOR DSTATCOM

In this section, design procedure of VSI parameters for Proposed DSTATCOM is explained. The VSI that need to be designed for better performance are DC-link Voltage (V_{dc}), DC-link storage capacitor (C_{dc}), switching frequency (f_{sw}), interfacing inductance (L_f), series capacitor (C_{se}) and shunt capacitor (C_{sh}). The procedure required to select these parameters is given below:

1) Selection of Reference DC-link Voltage (V_{dcref})

To achieve a good tracking performance, the voltage across DC capacitor needs to be selected carefully. The DC capacitor voltage should be greater than source phase voltage. It is observed that the DC-link voltage for split capacitor topology should be between 1.6 to 2 times of peak source voltage [17], [18]. In this study, the DC-link voltage value is taken as 1.6 times of peak value of the system voltage (V_m) for each capacitor. Consider a three-phase system with 230V line-to-neutral voltage. Hence for conventional DSTATCOM, the DC-link voltage across C_{dc} is maintained at,

$$V_{dcref} = 1.6 \times V_m = 1.6 \times \sqrt{2} \times 230 = 520\ V \qquad (1)$$

2) Selection of DC capacitor (C_{dc})

Once the DC-link voltage is obtained, the selection of DC-link storage capacitor is very important. The value of DC-link capacitor depends upon instantaneous energy available at DSTATCOM during transient period. The DC-link capacitor value is chosen as, [19]

$$C_{dc} = \frac{2(2S - S/2)nT}{(1.8V_m)^2 - (1.4V_m)^2} \qquad (2)$$

Where, S = KVA rating of the system

V_m= Peak value of source phase voltage

n = Number of cycles

T = Time period of each cycles.

Substituting the values of, V_m= $\sqrt{2}$ ×230 V, S = 15 kVA, *n*= 0.5 and *T*= 0.02 sec., C_{dc} is calculated as 3322 μF. In simulation studies, C_{dc} is taken as 3300 μF.

3) Selection of switching frequency for VSI (f_{sw})

The maximum switching frequency of VSI depends upon the type of switches used for higher switching frequency, MOSFET switches should be used, but their current and voltage ratings are lower as compared to that of IGBT switches. IGBT switches are preferred due to good switching speed and higher power handling capacity. Their maximum switching frequency is around 20 kHz.

4) Selection of interfacing inductance (L_f)

For tracking of reference currents, the interfacing inductance is selected from a trade-off which provides higher switching frequency and sufficient rate of change of filter current. The interfacing inductance is given by,

$$L_f = \frac{1.6V_m}{4hf_{swm}} \qquad (3)$$

Where, h = hysteresis band

Maximum switching frequency (f_{swm}) is assumed to be 10 kHz; and hysteresis band is taken as 0.5A. L_f is calculated to be 26mH.

5) Design of shunt capacitor (C_{sh})

In this study, load compensation with non-stiff source is considered. In the presence of such non-stiff source or weak source, PCC voltages and source currents get distorted. Also, PCC voltages get contaminated with the inverter switching frequency components. To eliminate these switching frequency components, a low impedance path is provided by filter capacitor C_{sh} connected in shunt at PCC, in each phase.

While designing the care is to be taken to avoid the resonance of shunt capacitor C_{sh} and feeder impedance L_s at fundamental frequency. If resonance occurs at a frequency ω_r, then we get,

$$C_{shr} = \frac{1}{{\omega_r}^2} \quad (4)$$

When ω_r is equal to fundamental frequency (say ω_0), let us assume that this capacitance is equal to C_{sh0}.So, to avoid resonance C_{sh} should never be chosen near C_{sh0}. This can be achieved by either $C_{sh}<<C_{sh0}$ or $C_{sh}>>C_{sh0}$. However, if we consider that $C_{sh}>>C_{sh0}$, the impedance between the PCC and ground will become very small. It will result in the excessive currents through filter capacitor. Therefore, the condition $C_{sh}>>C_{sh0}$ is invalid. Hence, we must restrict the value of C_{sh} to be much smaller than C_{sh0}.For feeder impedance L_s=0.01 H and fundamental frequency as 50 Hz, value of C_{sh0} is calculated around 1000 μF. Therefore, from condition $C_{sh}<<C_{sh0}$, we can choose C_{sh} as 50 μF.

But with increase in the value of C_{sh}, the system is pushed towards the series resonance and this also increases terminal voltages and source currents. Possible solution to this problem is the use of state feedback control to simultaneously force the terminal voltage and source current to be sinusoidal. This method is described in next section [20].

6) Design of series capacitor (C_{se})

The design of series capacitor C_{se} depends upon the value to which the DC-link voltage is reduced. The designing of C_{se} is carried out at minimum load impedance to ensure that the designed series capacitor C_{se} will perform satisfactorily at all loading conditions.

Let, S_{max} be the maximum kVA rating of a system and V_{base} is the base voltage of the system, and then the minimum impedance system is given as, $Z_{min} = \frac{{V_{base}}^2}{S_{max}} = R_l + jX_l$ (5)

$$I_{filter} = \frac{V_{inv1} - V_{t1}}{R_f + j(X_{Lf} - X_{Cse})} \quad (6)$$

$$I_{filter} = \frac{V_{inv1} - V_{t1}}{R_f + j(X_{Lf} - X_{Cse})} \quad (6)$$

And

$$I_{load} = \frac{V_{t1}}{R_f + jX_l} \quad (7)$$

Where,

$$X_{Lf} = 2\pi f L_f, \quad X_l = 2\pi f L_l, \quad X_{Cse} = \frac{1}{2\pi f C_{se}}$$

and$f$ is the supply frequency of fundamental voltage.

To achieve the unity power factor, the shunts filter current needs to supply the required load reactive current. This means that the imaginary part of shunt filter current should be equal to the imaginary part of load current. For this case, by neglecting the interfacing resistance we can write the equation as,

$$\frac{V_{t1}X_l}{{R_l}^2 + {X_l}^2} = \frac{V_{inv1} - V_{t1}}{(X_{Lf} - X_{Cse})^2}(X_{Lf} - X_{Cse}) \quad (8)$$

Where,

V_{inv1}= Line-to-neutral RMS voltage of inverter at the fundamental frequency

V_{t1}= Line-to-neutral RMS voltage of PCC at the fundamental frequency.

The equation of V_{inv1} in terms of DC-link voltage is given as follows [21]:

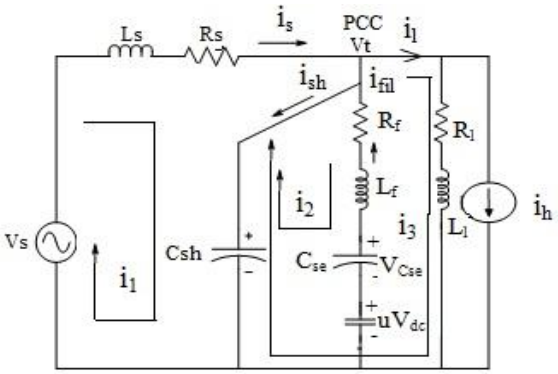
$$V_{inv1} = \frac{0.612V_{dc}}{\sqrt{3}} \quad (9)$$

The reason why we need to maintain the voltage across DC-link capacitor at a higher value than voltage at PCC is that basically the filter currents need to flow from inverter terminal to PCC. Due to this constraint, in various conventional DSTATCOM topologies the DC-link capacitor is rated at higher potential. Equation (10) represents the Kirchhoff's voltage law applied along the filter branch of proposed DSTATCOM as shown in Fig. 2.

$$R_f i_{fil} + L_f \frac{di_{fil}}{dt} = (uV_{dc} - V_{Cse}) - V_t \quad (10)$$

Where, u has the values ±1 depending upon inverter switching.

From equation (10), when the load is inductive in nature, the series capacitor voltage V_{Cse} gets added in terminal voltage of inverter uV_{dc}. This happens because when the load is inductive in nature the fundamental filter current lagsthe PCC voltage by $90^0$for reactive power compensation. Then the fundamental voltage across the filter capacitor again lags this filter current by 90^0. Eventually fundamental voltage across the capacitor will be in phase opposition to the PCC voltage. Thus, fundamental voltage across the capacitor gets added to the inverter terminal voltage. This will help to rate the DC-link capacitor voltage at lower value compared to that of conventional DSTATCOM topology. Therefore, for proposed



DSTATCOM the DC link voltage is chosen to be 300V.

Fig.2: Single phase equivalent circuit of Proposed DSTATCOM

TABLE I

SYSTEM PARAMETERS

Grid Parameters	Supply Voltage	Vs = 230v, 50 Hz
	Feeder Impedance	Z_s= 1+ j 3.141 Ω
Load Parameters	Linear Load	Z_{la} =34+ j 47.5 Ω Z_{lb} 814+ j 39.6 Ω Z_{lc} =31.5+ j 70.9 Ω
	Non-Linear Load	3-Ø Full Bridge Rectifier Load with R_{nl}=150 Ω &L_{nl}=300mH
VSI Parameters	V_{dcref} = 300V, C_{dc} = 3300 μF, L_f = 26 mH R_f = 0.1 Ω	
Series capacitor	C_{se} = 65 μF	
Shunt Capacitor	C_{sh} = 50 μF	
Voltage Controller (PI) Gains	K_p = 1, K_i = 0.2	
Hysteresis Band	h = ±0.5 A	

The system parameters for DSTATCOM are summarized in table I from which the minimum load impedance Z_{min} is taken as phase-*a*load impedance. From equation (8), the value of series capacitor is calculated as 65 μF.

CONTROL STRATEGY FOR DSTATCOM

The control strategy required for the proposed DSTATCOM mainly involves: (i) method to extract reference currents and (ii) current control strategy. For the generation of the reference currents instantaneoussymmetrical component theory (ISCT) and synchronous reference frame theory (SRFT) is used [22]-[25].

1) Instantaneous Symmetrical Component Theory

Using instantaneous symmetrical component theory (ISCT), the generated reference currents for phase *a* are given as follows:

$$I_{filt_a}{}^* = I_{la} - I_a$$

$$= I_{la} - \frac{V_{ta_1}{}^+ + \mu\left(V_{tb_1}{}^+ - V_{tc_1}{}^+\right)}{\left(V_{ta_1}{}^+\right)^2 + \left(V_{tb_1}{}^+\right)^2 + \left(V_{tc_1}{}^+\right)^2}\left(P_{avgl} + P_{swloss}\right) \quad (11)$$

Reference currents for phase b and c can be obtained similarly.
Where,
P_{avgl}= Average power of load.
P_{swloss} = Switching losses in compensator
And,

$$\mu = \tan\left(\frac{\psi}{\sqrt{3}}\right)$$

In the presence of feeder impedance, PCC voltages become distorted and unbalanced. Basically, if these voltages are unbalanced and distorted, it is not possible to draw sinusoidal currents with this compensation technique. This limitation overcomes by extracting fundamental positive sequence voltages at PCC as shown in equation (10).

2) Synchronous Reference Frame Theory

This control theory is based on the transformation of load currents in synchronously rotating frame. In this method, the three-phase measured load currents are transformed into d-q frame i.e. rotating frame, which is synchronously rotating at supply voltage frequency. This is represented by following equations (11) and (12):

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = \frac{\sqrt{2}}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & -\sqrt{3}/2 & \sqrt{3}/2 \end{bmatrix}\begin{bmatrix} I_{la} \\ I_{lb} \\ I_{lc} \end{bmatrix} \quad (12)$$

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} \quad (13)$$

Where, θ is the transformation angle.

The extracted DC components are obtained by using inverse Park's transformation as,

$$\begin{bmatrix} I_{\alpha_{dc}}{}^* \\ I_{\beta_{dc}}{}^* \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} I_{d_{dc}} \\ I_{q_{dc}} \end{bmatrix} \quad (14)$$

Now, by using inverse Clark's transformation, the reference currents are generated as follows:

$$\begin{bmatrix} I_a{}^* \\ I_b{}^* \\ I_c{}^* \end{bmatrix} = \frac{\sqrt{2}}{3}\begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} I_{\alpha_{dc}}{}^* \\ I_{\beta_{dc}}{}^* \end{bmatrix} \quad (15)$$

The Hysteresis Band Current Controller is used to compare the actual source currents with the reference current generated by the respective control algorithm. This controller generates switching commands for VSI switches. The switching logic for VSI is generated as follows:

$$u = hys\left[-K\{z - z_{ref}\}\right] \quad (16)$$

Where, the hysteresis function 'hys' is defined by,

If h ≥ +0.5 then hys (h) =1, lower switch is turned ON whereas the upper switch is turned OFF.

If h ≤ -0.5 then hys (h)=1, upper switch is turned ON whereas the lower switch is turned OFF.

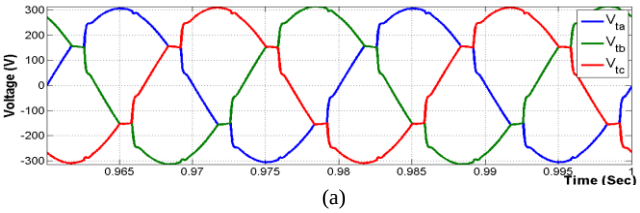
The upper and lower switches (IGBTs) are turned ON and OFF in a complementary fashion. Hysteresis Band Current Control (HBCC) is the fastest control method and its implementation is very simple. The main drawback of this method is that the converter switching frequency varies with the ac voltage.

SIMULATION RESULTS AND DISCUSSION

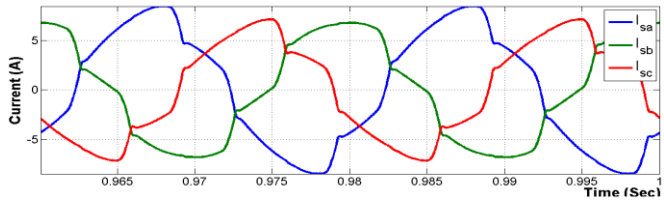
Simulation studies are carried out in order to validate the proposed DSTATCOM topology using MATLAB / SIMULINK software. The simulation results for both ISCT and SRFT control methods are presented in this section.

A. Distribution system without DSTATCOM

The performance of low voltage distribution system is demonstrated with unbalanced and non-linear loads. The system parameters (grid and load parameters) are to be considered as given in table I. In the presence of non-stiff source and non-linear load, terminal voltages and load currents get unbalanced and non-sinusoidal. Fig. 3 (a) and Fig. 3 (b) shows terminal voltages (PCC voltages) and load currents before compensation respectively.



(a)



(b)

Fig. 3: (a) Terminal voltages without DSTATCOM (b) Load currents without DSTATCOM

B. Distribution system with proposed topology of DSTATCOM

In this section, the simulation results of proposed hybrid DSTATCOM topology with two reference current generation methods i.e. ISCT and SRFT are presented. For simulation study the parameters of system given in table I are considered with controller gains as $K_{p=}2$ and K_i=0.5. ISCT and SRFT reference current generation techniques are described in Fig. 4 and Fig. 5 respectively.

The simulation results of hybrid DSTATCOM with ISCT technique is shown in Fig. 6. The source currents after compensation are shown in Fig. 6 (a). It can be observed that the source currents are free from switching components of inverter and are sinusoidal and balanced. Fig.6 (b) represents the filter currents after compensation. As described in section III, equation (10) shows that series capacitor voltage gets added in the DC-link capacitor voltage. Due to this, the voltage across both (upper and lower) DC-link capacitors can be maintained at 300V. It is depicted in Fig.6(c). Fig. 6(d) shows terminal voltages after compensation using hybrid DSTATCOM. The terminal voltages are seen to be free from inverter switching components and are balanced. The simulation results of proposed hybrid DSTATCOM topology with SRFT reference current generation method are shown in Fig.7. The source currents and filter currents after compensation are shown in Fig.7 (a) and Fig.7 (b), respectively. The DC-link capacitor voltages are shown in Fig.7 (c). Fig.7 (d) shows terminal voltages after compensation using hybrid DSTATCOM.

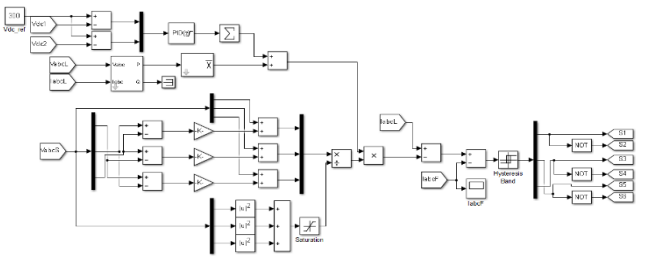


Fig. 4: Reference current generation using ISCT control method

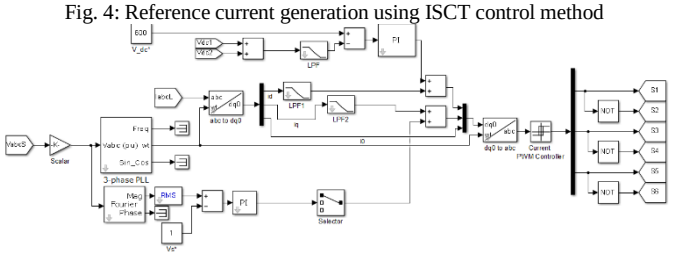
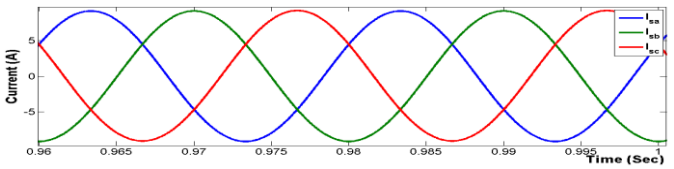
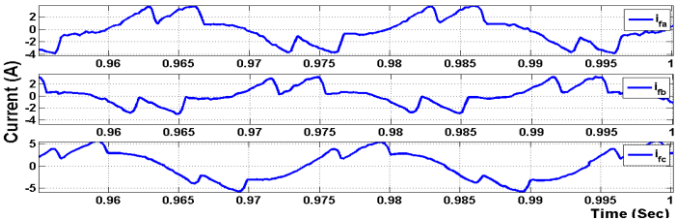


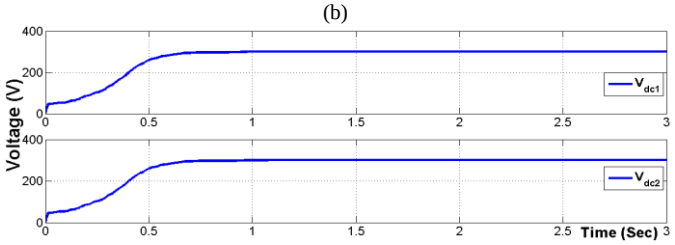
Fig. 5: Reference current generation using SRFT control method



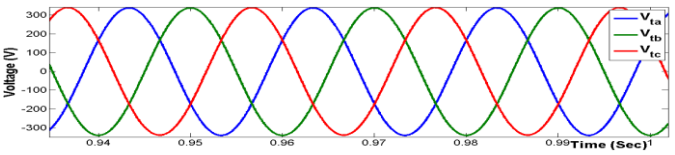
(a)



(b)



(c)



(d)

Fig. 6: Simulation results using ISCT reference current generation method (a) Compensated source currents (b) Compensated filter currents (c) DC-Link capacitor voltages (upper and lower) (d) Terminal voltages after compensation

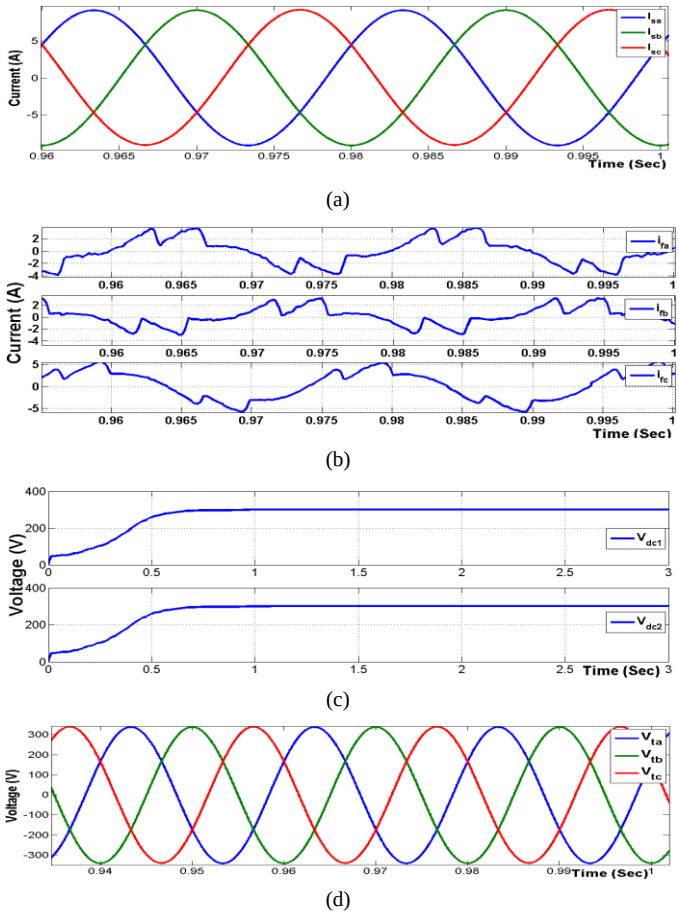


Fig. 7: Simulation results using SRFT reference current generation method (a) Compensated source currents (b) Compensated filter currents (c) DC-Link capacitor voltages (upper and lower) (d) Terminal voltages after compensation

TABLE II

THD OF TERMINAL VOLTAGES AND SOURCE CURRENTS

Parameters	THD (%)		
	Without DSTATCOM	With DSTATCOM	
		Conventional topology (ISCT)	Proposed topology (SRFT)
V_{ta}	7.49	0.27	0.21
V_{tb}	7.2	0.29	0.23
V_{tc}	7.49	1.01	0.7
I_a	11.11	0.62	0.56
I_b	12.48	0.73	0.63
I_c	13.64	1.35	1.23

From Fig.6 and Fig.7 it can be observed that, similar results of hybrid topology are obtained with slight improvement in THD values. The THD values of terminal voltages and source currents are listed for distribution system with and without DSTATCOM and summarized in table II.

CONCLUSION

The terminal or PCC voltages and source currents get distorted due to the inverter switching in presence of non-stiff source. Load compensation of low voltage distribution system with non-stiff source using DSTATCOM is presented in this paper. The hybrid DSTATCOM topology can reduce the voltage of DC-link capacitor at a lower value than conventional DSTATCOM topology. The design of components of hybrid DSTATCOM is explained in detail. The two control strategies ISC theory and SRF theory have been employed to demonstrate performance of DSTATCOM. Comparative study of distribution system with ISCT and SRFT control methods are made. The simulation studies indicate that hybrid DSTATCOM topology with SRFT control method has less THD in terminal voltages and source currents as compared to hybrid DSTATCOM topology with ISCT control method.

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