Asian Journal of Convergence in Technology Volume IV Issue I
ISSN NO: 2350-1146 I.F-5.11

High Performance Arithmetic and Logic Unit with Enhanced MTCMOS and Transistor Stacking Techniques

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***Abstract*—Short channel devices need lower power supply voltages to reduce power consumption. This forces a reduction in the threshold voltage that causes a substantial increase of weak inversion current. The popular leakage control technique is Multi Threshold Complementary Metal Oxide Semiconductor (MTCMOS) technique. Power gating uses a pMOS transistor and/or an nMOS transistor to disconnect supply voltage from the logic when the logic is inactive by creating virtual V_{DD} and Ground. This technique can decrease leakage power by more than 50% with negligible delay. For further reduction in the leakage power in deep submicron, a technique known as Enhanced MTCMOS (EMTCMOS) is used which uses a stack of NMOS and PMOS transistors as used in case of MTCMOS technique. EMTCMOS technique condenses leakage further, over the conventional MTCMOS circuits. Transistor stacking is another technique that is verified for leakage power reduction. An Arithmetic and Logic Unit is designed using CMOS, MTCMOS, EMTCMOS and Transistor stacking techniques and compared for the leakage power reduction**

Keywords—Short Channel; Leakage Power; MTCMOS; EMTCMOS; Transistor Stacking, Arithmetic and Logic Unit;

I. INTRODUCTION (*HEADING 1*)

In days to come, it understood that a microprocessor, clocked at 500 MHz with 10cm² chip area may consume about 300W. The cost allied with packaging and cooling of such devices is very high. As the essential power consumption must be dissipated through the expensive packaging and also cooling strategies are essential as chip power consumption increases. Peak power known as maximum possible power dissipation is a important design factor because it determines the thermal and electrical limits of designs and further impacts the system size there by cost, weight based on battery type, system packaging, heat sinks and overstates the resistive and inductive voltage drop problems. It is therefore essential to have the peak power under control.

From the environmental viewpoint, the smaller the power dissipation of electronic systems, the lower the heat pumped into the rooms, the lower the electricity consumed and therefore, the less the impact on global environment. For high performance, in portable computers such as laptops and notebook computers, the goal is to reduce the power dissipation of the electronics portion of the system to a point which is about half of the total power dissipation. Finally, for high performance, the overall goal of power minimization is to reduce system cost and ensure long-term circuit reliability. Low-power design is not only essential for portable applications but also for high-performance systems.

I. DESIGN OF CMOS OF ARITHMETIC AND LOGIC UNIT

The Arithmetic Logic Unit (ALU) is one of the core components inside a microprocessor and responsible for performing arithmetic and logic operations. The ALU is a vital building block of the Central Processing Unit (CPU) of a computer, and even the simplest microprocessors contain one. The processors found inside modern CPUs and Graphics Processing Units (GPUs) have inside them very powerful ALUs.

Typically, the ALU has direct input and output access to the processor controller, Random Access Memory (RAM) in a personal computer, input/output devices and input and output data in a bus. As per the selection input, the Multiplexer will select corresponding operation and that operation is performed by ALU. ALU has four major components. Arithmetic block performs the core of the arithmetic block is the adder. Logic block performs simple bitwise logic operations. Multiplexers are used to select the appropriate inputs for the arithmetic and logic blocks. Registers can be used to store the data and the results [5]. The ALU designed by using multiplexers and full adder circuit. The multiplexers are designed based on Boolean expression in CMOS design where as full adder circuit is designed with 10-transistors [1,2].

A. ALU Design and Operation

4-bit ALU has been designed with for a supply voltage of 1V. The ALU has four stages, each stage consisting of three parts: 1) input multiplexers 2) full adder and 3) output multiplexers as shown in figure 1. The ALU performs four arithmetic and four logical operations. The input and output sections consist of 4x1 and 2x1 multiplexers. The multiplexers are designed using the pass transistor logic. A set of three select signals have been incorporated in the design to determine the operation being performed and the inputs being selected[7,8].

The 4-bit ALU was designed using 90nm, n-well CMOS technology. The INCREMENT and DECREMENT operations logic '1' and logic '0' are applied as inputs respectively. The complement of B input is used for SUBTRACTION. The full adder completes the SUBTRACT operation by two's complement method. An INCREMENT operation is performed by adding '1' to the addend and DECREMENT is the subtraction of 1from the input and is shown in table 1.

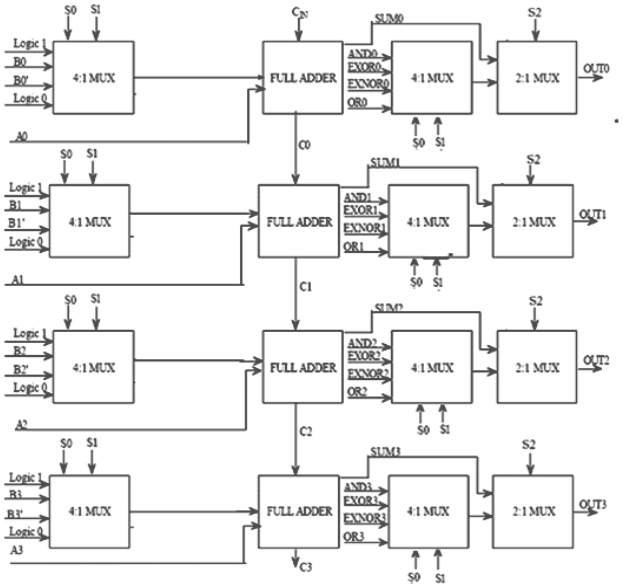


Figure 1: Block diagram of a 4-bit ALU.

Table 1 ALU Operations

S2	S1	S0	Operation
0	0	0	Addition
0	0	1	Subtraction
0	1	0	Increment
0	1	1	Decrement
1	0	0	AND
1	0	1	EXOR
1	1	0	EXNOR
1	1	1	OR

B. Full Adder Design

In ALU, full adder is the essential component of the entire design of ALU especially in this architecture. The full adder performs the arithmetic operations of ALU. One of the outputs of full adder SUM is connected to the input of multiplexer and carry will be sent to the carry bit of the full adder in the next stage. As per selection input signals, the multiplexer stage selects the appropriate inputs and gives it to the full adder. The full adder computes the results. The multiplexer at the output stage selects the appropriate output and sends it out. All the multiplexers have been implemented using pass transistors, but the full adder has been implemented using 10-transistors which include both NMOS and PMOS transistors[4,5].

A full adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. In this design, the three inputs are A, B and C_{in}. The input C_{in} denotes carry input in the first stage. The Boolean expressions for the SUM and CARRY bits are as given below.

$SUM= AB'C_{in}'+A'BC_{in}'+A'B'C_{in} +ABC_{in}$ (1)

$CARRY= AB + AC_{in} + BC_{in}$ (2)

Figure 2 shows the 10 transistor full adder used in the implementation of ALU. This type of circuits have no static and short circuit power dissipation as it does not have complementary pull-up and pull-down circuits [5,6]. Figure 3 shows schematic diagram of CMOS 8-bit ALU, which consists of two 4-bit ALUs.

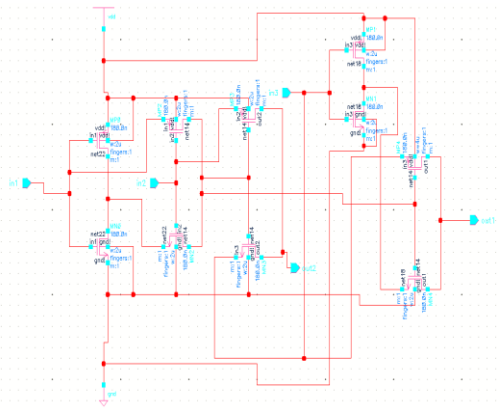


Figure 2: Schematic of a 10 transistor full adder.

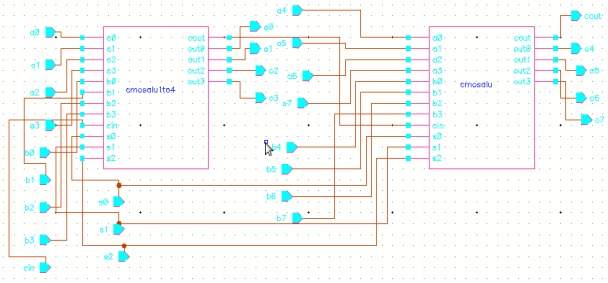


Figure 3. Schematic of CMOS 8-bit ALU

II. LOW POWER TECHNIQUES

A. *DYNAMIC POWER REDUCTION TECHNIQUES*

The quadratic relationship between dynamic power consumption and V_{DD} conveys that reducing the supply voltage is the most effective way to lower the dynamic power, but gate delay increases. To avoid performance degradation, threshold voltage drop proportional to the supply voltage is necessary so that a sufficient driving current is maintained. The drop in threshold voltage causes an exponential increasing in leakage power, further raises the static power of the device to unacceptable levels. In general, gates of the critical paths operate with higher V_{DD} or lower V_{th} and gates on non-critical paths operate at the lower V_{DD} or higher V_{th}. Thus total power dissipation is upheld without performance degradation. Power supply scaling also needs support circuitry for low-voltage operation including level-converters and DC/DC converters as well as detailed consideration of issues such as signal-to-noise margins[13].

The power savings that can be achieved by various static and dynamic power management techniques are very application dependent and sometimes substantial. These methods relate with one another in terms of CMOS device scaling or supply voltage scaling. The selection of architecture must be done sensibly and carefully to find an optimum power-area-delay trade-off [3,9].

B. *LEAKAGE OPTIMIZATIONTECHNIQUES*

Many circuit techniques targeting the reduction of leakage power have appeared in the literature. Most of these techniques target the circuits during the standby operation mode and some target the circuits during the active mode of operation. Few techniques mostly aim to reduce sub-threshold leakage current while others tend to reduce gate leakage current. Transistor stacking, Multi-Vth, Dynamic Vth, Supply Voltage Scaling, Input Vector Control, Body Biasing are the existing techniques for leakage power reduction. A PMOS sleep transistor is used along with body bias and clock gating techniques to reduce the leakage power. A low block reactivation time after exiting the sleep mode is also maintained[11].

i. Transistor stacking techniques

All the above-mentioned techniques are applicable when there are two or more stacked transistors which are switched OFF. Sub-threshold leakage current reduces using transistor stacking in two ways. It rises the source bias of upper transistors in the stack and lowers the gate-to-source voltages of these transistors. This results in a lower sub-threshold leakage current. Reduction of leakage using transistor stacks depends on the choice of input pattern during standby periods since it determines the number of OFF transistors in the stack. Leakage current dependencies on circuit state can be exploited and used to determine a low leakage state by using a heuristic search algorithm to find the minimum leakage input vector, which is fed into the circuit during sleep mode.

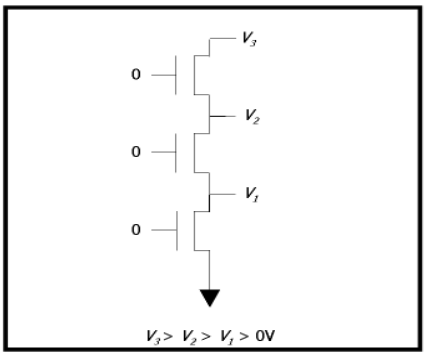


Figure 4: The effect of transistor stacks in reducing I_{sub}

After this input vector is found, the circuit is evaluated and additional leakage control transistors are inserted in the non-critical paths where only one transistor is originally turned OFF. Figure 4 shows the transistors in stack[12].

Sub-threshold leakage current that is flowing through a stack of series-connected transistors decreases when more than one transistor in the stack is turned off. This effect is known as the "stacking effect" or "self reverse bias". Leakage currents in NMOS or PMOS transistors depend exponentially on the voltage at the four terminals of transistors. When V_G is '0', V_S of NMOS transistor increases and reduces sub-threshold leakage current exponentially. A stack of two NMOS transistors as shown in the Figure 5[17,18].

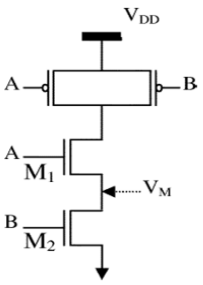


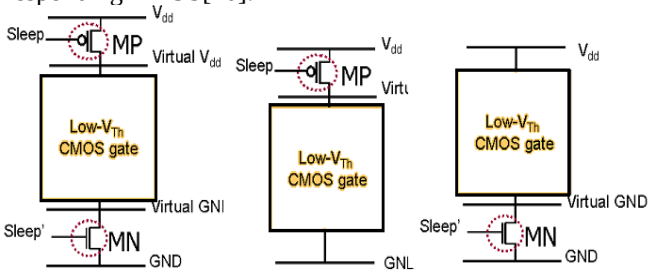
Figure 5: Effect of transistor stacking on source voltage.

ii. Multi-Vth techniques

A far more aggressive and effective technique for leakage mitigation is to simply cut the power supply to any inactive transistor. Simply by placing MOS switches in the power network, the ground network or both this is done. The exact sizing and placement of these switches must be done to avoid an adverse impact on performance. This is the most common approache to reduce leakage currents where two different types of transistors are fabricated on the chip. Based on the multi-threshold techniques previously described, several multiple-threshold circuit design techniques have been developed[14-16].

iii. Multi-threshold voltage CMOS

Advanced CMOS technology can enable high levels of performance with reduced active power at the expense of increased standby leakage, MTCMOS has previously been described as a method of reducing leakage in standby modes. Reduce the leakage by inserting high-threshold devices in series to low Vth circuitry. Figure 6 (a) shows the schematic of an MTCMOS circuit. In the active mode, Sleep is set to low and sleep control to high Vth transistors (MP and MN) are turned on. As the on-resistance is small, the virtual supply voltages (Virtual Vdd and Virtual GND) almost function as real power lines. In the standby mode, Sleep is set to high, resulting MN and MP to turn off, and the leakage current reduces. Only one type of high Vth transistor is enough for leakage control. Figure 6 (b) and (c) show the PMOS insertion and NMOS insertion schemes, respectively. The NMOS insertion method is preferable, since the NMOS on-resistance is smaller at the same width. NMOS can be sized smaller than corresponding PMOS[10].



(a) (b) (c)

Figure 6: MTCMOS Technique (a) pMOS and nMOS sleep devices (b) pMOS Sleep device in the pull-up (c) nMOS sleep device in the pull-down

iv. Enhanced MTCMOS

In an enhanced MTCMOS, sub-threshold leakage is reduced in sleep mode due to the added effect of stacking of high threshold voltage transistors. Maximum savings in sub threshold leakage are obtained if the devices in the stack are sized as:

$W_0 = W/(1-\alpha)$ (3)

$W_1 = W/\alpha$ (4)

Where $\alpha=\lambda/(1+2\lambda)$

the lower device in the stack is bigger than the upper device, an increased negative gate-to-source bias and a reduced drain-to-source bias (i.e. reduced DIBL) for the upper device resulting in reduced sub-threshold leakage.

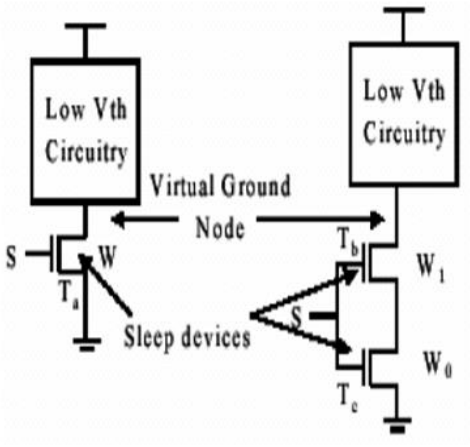


Figure 7: Enhanced MTCMOS technique

Enhanced MTCMOS circuit is shown in figure 7. The average gate leakage is always greater than that for the MTCMOS configuration. The stacked sleep devices can also be sized to maximize the savings in gate leakage factor as

$W0 = W(1+\beta)$ (5)

$W1 = W[(1+\beta)/\beta]$ (6)

Thus the lower device is required to be bigger than the upper ones a lower gate leakage in the off state optimizing for gate leakage is nearly identical to optimizing for total leakage[19].

III. ALU USING MTCMOS, ENHANCED MTCMOS AND TRANSISTOR STACKING

A. Implementation of ALU using MTCMOS

All the blocks of ALU of 2x1 Mux, 4x1 Mux and Full adder are designed using fine grain MTCMOS technique. Figure 8 shows the Inverter using MTCMOS technique. Performance of the ALU can be increased, by reducing the static power dissipation in the circuitry. Figure 9 shows the schematic of 8-bit ALU using MTCMOS. The power dispassion is very less for this ALU when compared to ALU in CMOS implementation.

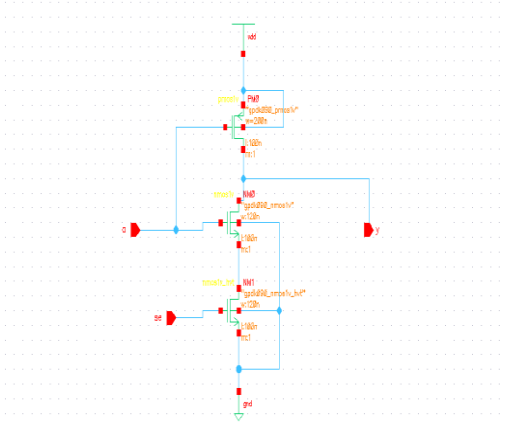


Figure 8: Inverter using MTCMOS technique

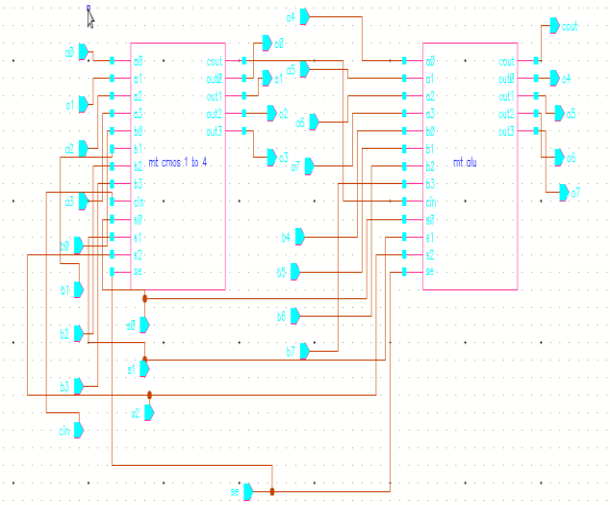


Figure 9: 8-Bit ALU using MTCMOS

B.Implementation of ALU using EMTCMOS

In an enhanced MTCMOS configuration, sub-threshold leakage is reduced in sleep mode due to the added effect of stacking of high threshold voltage transistors. Maximum savings in sub threshold leakage are obtained if the devices in the stack are properly sized. The lower device in the stack is bigger than the upper device. Figure 10 and Figure 11 shows the EMTCMOS Inverter and the 8-bit ALU implemented using EMTCMOS technique respectively.

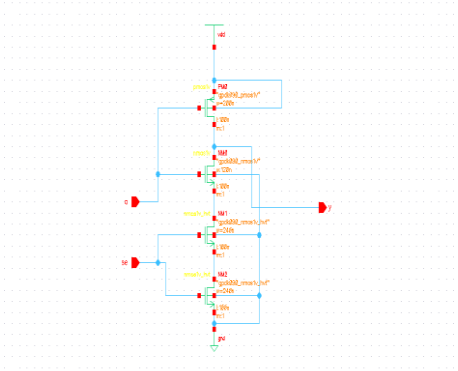


Figure 10: EMTCMOS Inverter

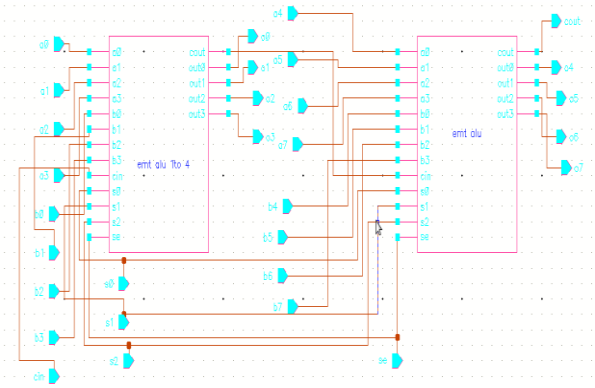


Figure 11: 8-Bit ALU using EMTCMOS Technique

C.Implementation Using Transistor Stacking

Sub-threshold leakage current that is flowing through a stack of series-connected transistors decreases when more than one transistor in the stack is turned off. This effect is known as the “stacking effect” or “self reverse bias”. Leakage currents in NMOS or PMOS transistors depend exponentially on the voltage at the four terminals of transistors. Figure 12 and Figure 13 shows the Inverter using transistor stacking and the 8-bit ALU implemented using transistor stacking technique respectively.

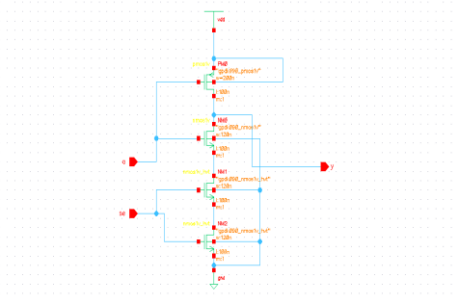


Figure 12: Inverter using Transistor stacking

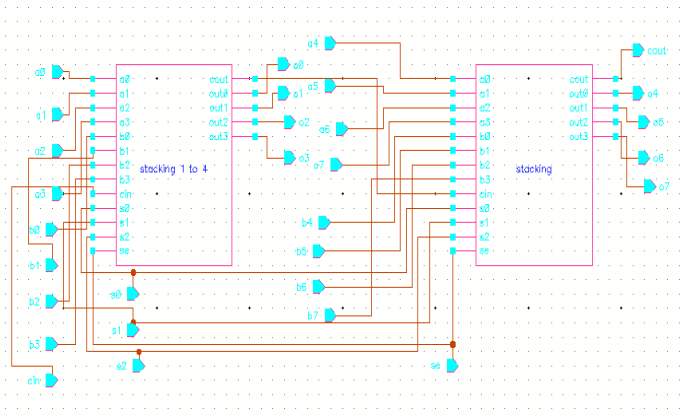


Figure 13: Transistor stacking 8-Bit ALU

IV. RESULTS

Testing environments to check the static and dynamic performance are set up. Though speed is not a major concern in this work, by knowing the conversion time it is convenient to measure the design margin in terms of power and speed. Table 2 and 3 shows the power consumption and the transistor count for an 8-bit ALU. All the eight operations including four arithmetic and four logical operations are verified. ALU implemented using MTCMOS, EMTCMOS and Transistor stacking techniques are also verified and the outputs are observed to be correct. Figure 14 shows the simulation results of 8-bit ALU using three different leakage power reduction techniques.

Table 2 Power consumption of individual cells of ALU

Module	CMOS	MTCMOS	Transistor Stacking	EMTCMOS
Inverter	58.3ηW	550pW	453 pW	535 pW
NAND	81.6 ηW	1.7 ηW	1.6 ηW	1.72 ηW
NOR	80.5 ηW	3.77 ηW	3.6 ηW	3.74 ηW
AND	256 ηW	1.36 ηW	1.3 ηW	1.391 ηW
OR	157 ηW	2.67 ηW	2.57 ηW	2.5 ηW
XOR	487 ηW	6.6 ηW	5.96 ηW	6.05 ηW
XNOR	575 ηW	4.07 ηW	3.75 ηW	3.75 ηW
2X1 MUX	364 ηW	6.65 ηW	3.03 ηW	3.05 ηW
4X1 MUX	1.67 µW	16.7 ηW	14.66 ηW	15.02 ηW
Full Adder	3.8 µW	8.02 ηW	7.4 ηW	7.5 ηW
8-Bit ALU	55.93 µW	26.38 µW	16.85 µW	16.85 ηW

Table 3 Transistor count for the individual cells of ALU

Module	CMOS	MTCMOS	Transistor Stacking	EMTCMOS
Inverter	2	3	4	6
NAND	4	5	6	6
NOR	4	5	6	6
AND	6	8	10	10
OR	6	8	10	10
XOR	12	15	18	18
XNOR	14	18	22	22
2X1 MUX	12	18	22	22
4X1 MUX	36	54	66	16
Full Adder	42	54	66	16
8-Bit ALU	42	54	74	74

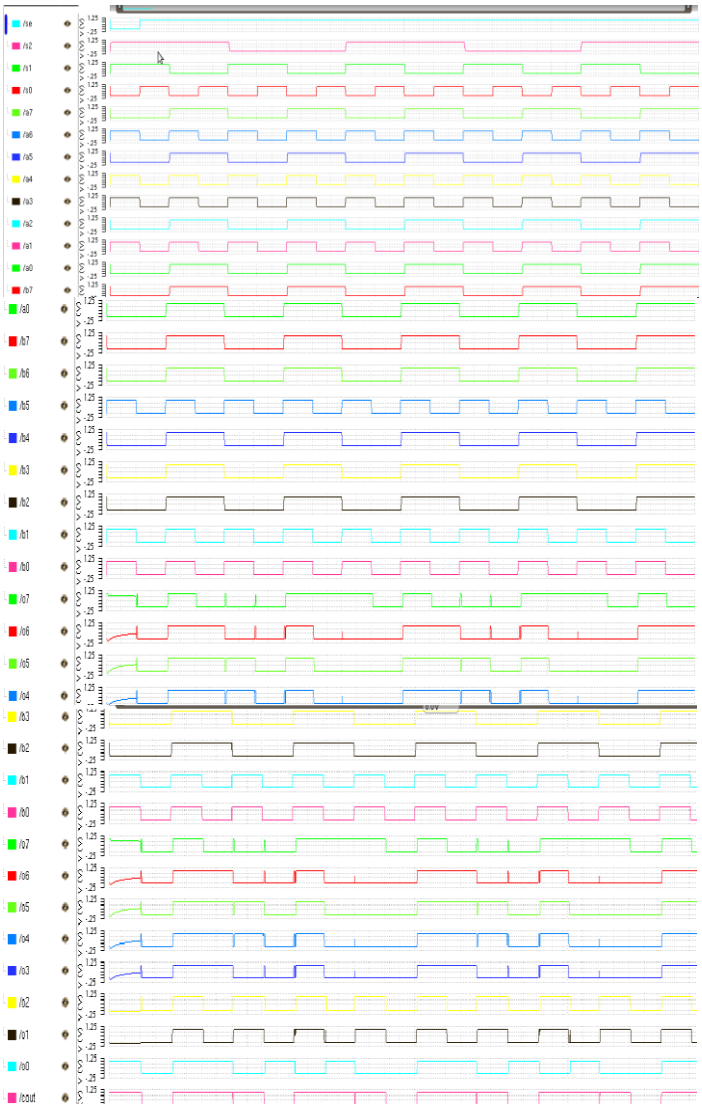


Figure 14: Simulation of 8-Bit ALU

CONCLUSION

In this work, an ALU is designed at transistor level using Virtuoso Schematic Editor and simulated using ADEL of Cadence tools. ALU results show that low power and minimum area with good performance is achieved. For large number of computations efficient ALU is to be designed for minimum area and low-power without compromising the high speed. The power consumption of 8-bit ALU is observed to be 26µw for MTCMOS, 16µw for transistor stacking and 16µw

for EMTCMOS. The ALU can be designed for higher bit inputs also. Using this ALU as component, any low power DSP applications can be constructed. Some glitches are observed in the simulation results which consumes extra power. This also can be reduced by considering extra circuitry. Other leakage power reduction techniques can also be compared.

Acknowledgment (HEADING 5)

The authors would like to thank the University Grants Commission, New Delhi, India for sponsoring the research work and CVR College of Engineering for providing infrastructural facilities

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