A Simulation Study of a Three Phase Five Level Diode Clamped Inverter with LCL filter for Solar PV based Grid-tied Application

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Abstract— **Solar energy is now increasingly being harnessed to fulfill the load requirements of modern power grid. Power converters are employed to convert DC output of a Solar PV array to AC for grid connection. Major factors considered for selection of converters for PV system are efficiency, reliability and cost of the system. Use of multilevel inverters for such applications can enhance the efficiency of the system by reducing losses in the power conversion stage and by improving total harmonic distortion. This paper presents a study on a three phase five level diode clamped inverter for Solar PV based grid-tied application. The main advantage of this topology is its simplicity of control, reduced stress on individual switches and cost effectiveness. Moreover, effect of LCL filter on the output of these multilevel inverters is observed. The Incremental Conductance MPPT algorithm is used to extract maximum power from the DC-DC converter. The 110kW PV system model is developed and simulated using MATLAB/SIMULINK to verify the performance of the inverter.**

Keywords— *Multilevel inverter (MLI), Five-Level, Diode Clamped, Solar Photovoltaic (PV), Grid-Tied Inverter, LCL Filter, THD*

I. INTRODUCTION

In recent years, solar photovoltaic (PV) energy generation has become increasingly popular and is an integral part of modern day grid. A typical system consists of a PV array, a MPPT based DC-DC converter, an inverter and grid utility. A block diagram of the system is shown in Fig. 1.
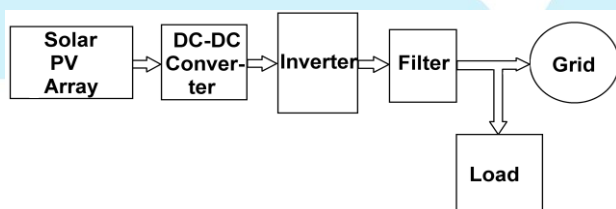

Fig. 1. Block Diagram of Solar PV Grid Tied System

Major factors that affect overall efficiency of the system are efficiency of the PV array and inverter. Usually PV array has efficiency ranging between 6-22% [1] which is quite low.

Therefore, by improving the efficiency of the grid connected inverter, the efficiency of the PV system can be improved.

A conventional two-level voltage source inverter produces a square wave output which is not suitable for most of the intricate applications and a pure sinusoidal waveform is desired [2]. On the other hand, multilevel inverters generate more voltage steps in the output voltage nearly producing sinusoidal voltage thereby reducing the total harmonic distortion [3]. According to their topology, voltage source multilevel inverters are categorized as: diode clamped (neutral point clamped), flying capacitor (FLC) and cascade H-bridge [4]–[8]. A diode clamped topology has advantages like common DC-link capacitors to three phases, can operate even on low switching frequency and gives control over reactive current and negative phase sequence current [9], [10]. Moreover, this topology is easier to design and implement and is hence widely used for practical applications [11].

As inverters are operated at high switching frequency using different PWM techniques, they generate switching harmonic components in output current [12], [13]. A low pass filter is used to filter out these current ripples [14], [15]. Usually an inductor (L) is used for this purpose [16]. However, a LC or LCL configuration of filter needs to be used to meet international standards regarding harmonic content in grid connected systems [17]- [21].

The effect of LCL filter configurations on a three phase five level diode clamped Solar PV grid tied inverter is studied and presented in this paper along with a comparative analysis of THD between a conventional two level, a three- level diode clamped and a five-level diode clamped inverter. This paper is organized as follows: Introduction section is followed by discussion of the basic operation of a three phase five level diode clamped inverter in Section II. Section III presents a study on LCL filter configuration for reducing the harmonic content in inverter voltages and currents before they enter the grid. Section IV consists of simulation and its results for the proposed multilevel inverter configuration in a 110kW solar PV system and section V concludes the paper.

II. THREE PHASE FIVE LEVEL DIODE CLAMPED INVERTER

A three phase five-level diode-clamped inverter is shown in Fig. 2. It consists a total of 24 IGBT switches (8 in each leg) and 18 diodes (6 in each leg).
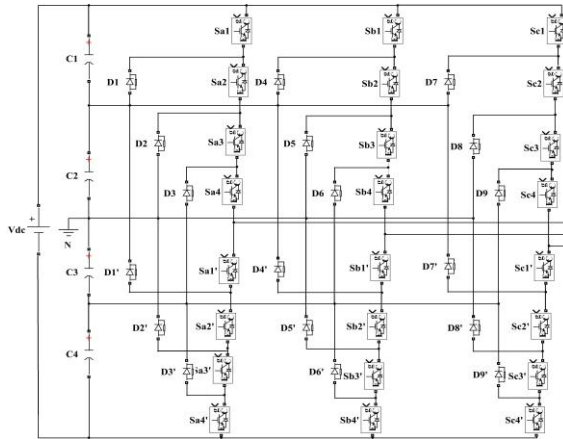

Fig. 2. Three Phase Five Level Diode Clamped Inverter

In this circuit, four capacitors C_1 to C_4 divide the DC bus voltage into five voltage levels $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$ and $-Vdc/2$ as referred to the neutral point N. The middle point between C_2 and C_3 capacitors is defined as the neutral point N. The switching pattern for the inverter is presented in Table I.

TABLE I

VOLTAGE LEVELS AND SWITCHING PATTERN FOR THREE-PHASE FIVE LEVEL DIODE CLAMPED INVERTER FOR PHASE A

Voltage Levels (V_{an})	Switching state							
	Sa1	Sa2	Sa3	Sa4	Sa1'	Sa2'	Sa3'	Sa4'
Vdc/4	0	1	1	1	1	0	0	0
Vdc/2	1	1	1	1	0	0	0	0
0	0	0	0	1	1	1	0	0
-Vdc/2	0	0	0	0	1	1	1	1
-Vdc/4	0	0	0	1	1	1	1	0

The main difference between a conventional two-level inverter and the five-level topology is the inclusion of 18 diodes. These diodes clamp the voltage to half and quarter level of the dc-bus voltage at appropriate nodes. For a given dc-bus voltage V_{dc}, the voltage stress across each individual capacitor is limited to $V_{dc}/4$ through these clamping diodes.

To improve utilization of DC voltage and to reduce conduction and switching losses, sinusoidal pulse width modulation (SPWM) is a widely used technique for switching of power devices in an inverter. In this technique, a sinusoidal reference signal is compared with a high frequency triangular carrier signal to generate gate pulses for the power switches of the inverter. The frequency of the inverter output is determined by the frequency of the modulating sinusoidal signal.

Phase Dissipation (PD) is a popular vertical carrier distribution technique used to improve the performance of diode clamped inverters [7]. In this technique, a high frequency triangular carrier signal of equal amplitude is generated and compared with a sinusoidal reference signal to generate gate pulses for the inverter. A PD method for generating gate pulses for phase *a* of a five-level diode clamped inverter is shown in Fig. 3 and output phase voltage V_{an} of the inverter for $V_{dc} = 400V$ is shown in Fig. 4.
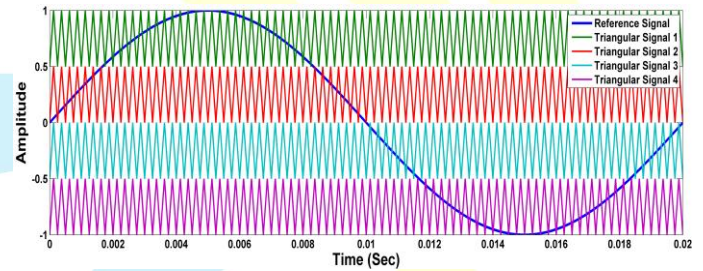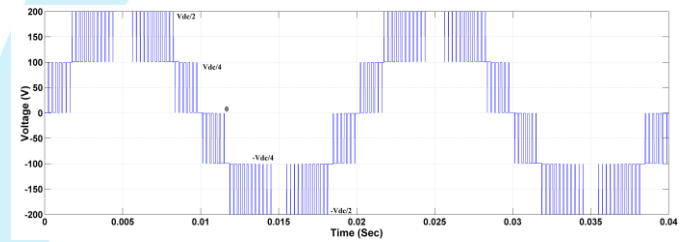

Fig. 3. SPWM using phase dissipation (PD) method

Fig. 4. Output Phase Voltage of Five Level Diode Clamped Inverter

III. GRID CONNECTED LCL FILTER

A simple L filter has low efficiency for suppression of current harmonics. To improve its performance large inductors will be required which are not desirable. Therefore, LCL filter configuration is suggested for grid tied applications as attenuation of high frequency components can be better achieved even with small inductors. A typical solar PV grid-connected inverter with LCL filter is shown in Fig. 5 and its equivalent single-phase circuit is shown in Fig. 6.
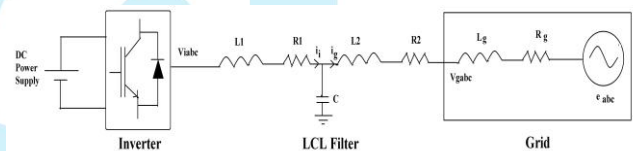

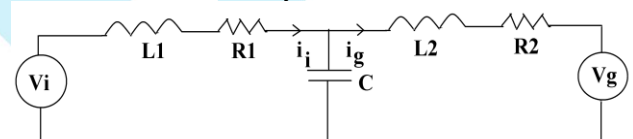Fig. 5. Schematic Diagram of a grid-connected inverter in solar PV system

Fig. 6. Equivalent Circuit Diagram of a LCL filter

The state equations in dq synchronous reference frame can be written as [16]:

$$\frac{di_{i-dq}}{dt} = \frac{v_{i-dq}}{L_1} - \frac{v_{c-dq}}{L_1} - \frac{R_1 i_{i-dq}}{L_1} - j\omega_g L_1 i_i - dq \quad (1)$$

$$\frac{di_{g-dq}}{dt} = \frac{v_{c-dq}}{L_2} - \frac{v_{g-dq}}{L_2} - \frac{R_2 i_{g-dq}}{L_2} - j\omega_g L_2 i_g - dq \quad (2)$$

$$\frac{dv_{c-dq}}{dt} = \frac{i_{i-dq} - i_{g-dq}}{C} - j\omega_g v_c - dq \quad (3)$$

Where,

$w_g = 2\pi f_g$,

fg = grid frequency,

v_i and i_i are inverter voltage and current,

v_c is the voltage across filter capacitor,

v_g and i_g are grid voltage and current.

All variables are written in dq-frame and represented in $d+jq$ form. The block diagram of a typical LCL filter according to (1) - (3) is shown in Fig. 7.
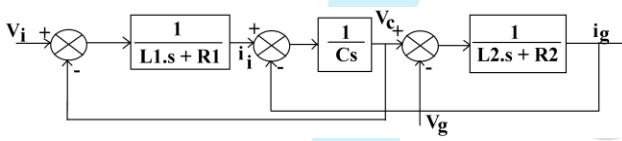

Fig. 7. Block Diagram representation of LCL filter

A. Design procedure of LCL filter

Grid frequency, rated power and voltage (L-L) determine the components of filter. The factors considered for the design of LCL filter are current ripple, reduction in amplitudes of harmonic components and filter size.

Inductor on inverter side (L_1) is calculated by the criteria of output current ripple. If maximum output current ripple ΔI_{Lmax} is known, then value of inverter side inductor L_1 is given by [16]

$$L_1 = \frac{V_{dc}}{6\Delta I_{Lmax} - f_{sw}} \quad (4)$$

Where,

$\Delta I_{Lmax} = \frac{2V_{dc}}{3L_1 f_{sw}} (1 - m)m$,

m = modulation index between 0 and 1,

V_{dc} = DC voltage,

f_{sw} = switching frequency.

The value of capacitor (C) is calculated based on maximum permissible variation in reactive power (typically, 5-7.5%) at the point of common coupling (PCC) and is given as [22]

$$C_f = 0.05 C_{base} \quad (5)$$

The output current ripple attenuation is given as [16]

$$K_a = \frac{1}{|1 + r[1 - L_1 C w_{sw}^2]|} \quad (6)$$

Where,

$$r = \frac{r_2}{r_1}$$

The relationship between K_a and r is shown in Fig. 8. Accordingly, by choosing a suitable value for K_a, r is determined. Then value of grid side inductor L_2 is given as [16]
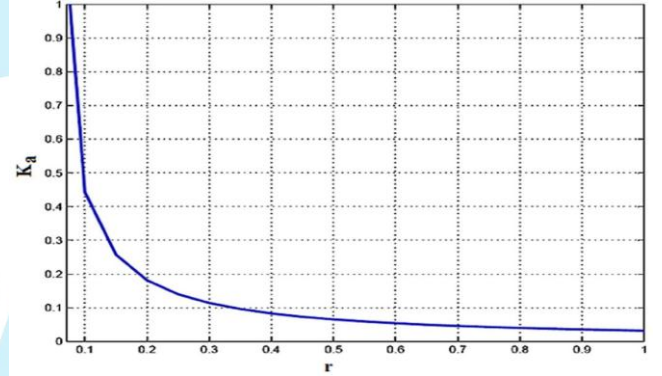
$$L_2 = rL_1 \quad (7)$$

Fig. 8. Plot of attenuation factor (K_a) versus r

B. Frequency Response of LCL filter

The transfer function of a LCL filter is

$$\frac{i_g}{V_{inv}} = \frac{1}{L_1 L_2 C s^3 + (L_1 L_2)s} \quad (8)$$

Fig. 9 shows Bode plot wherein a peak is seen to occur at resonance frequency of LCL filter. This may lead to oscillations and cause instability of the system. Hence a small damping resistor is employed in series with L_1 to damp the resonance oscillations.
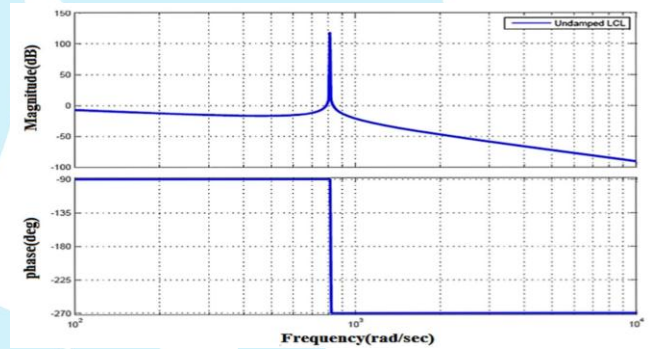

Fig. 9. Bode plot for transfer function of LCL filter

IV. SIMULATION MODEL AND RESULTS

The Simulink model of power circuit of three phase five level diode-clamped grid connected inverter is shown in Fig. 10. A 110kW system is simulated in MATLAB/Simulink environment.
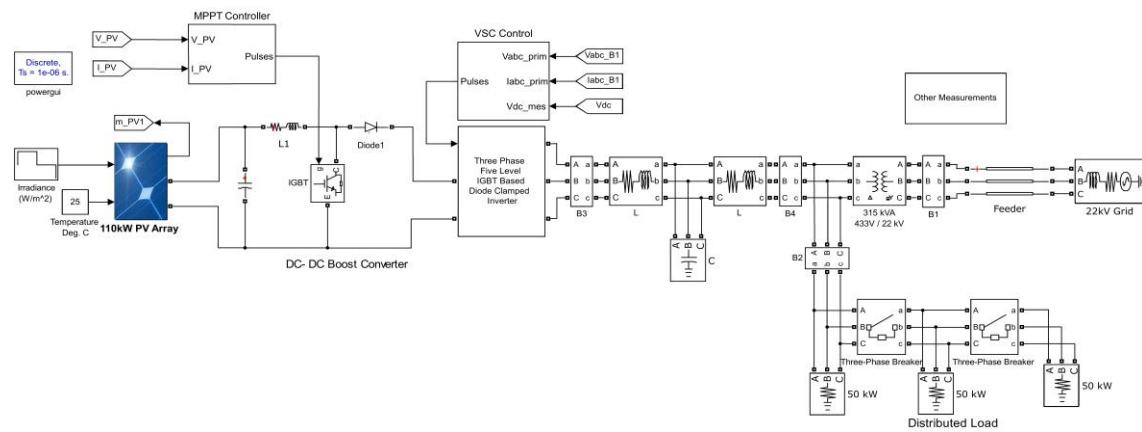
Fig. 10.   Simulink model of 110kW Solar PV Grid-Tied Three Phase Five Level NPC Inverter

The specifications of the proposed system are given in Table II.

TABLE II
DESIGN PARAMETERS OF PV SYSTEM

Parameters	Symbol	Specification
PV Array		110kW
DC-link Capacitor	C_{dc}	$2200\mu F \times 4$
DC-link Voltage	V_{dc}	500V
Grid Frequency	f_g	50Hz
Inverter Side Inductor	L_1	2.5mH
Grid Side Inductor	L_2	0.5mH
Filter Capacitor	C	100mF
Damping Resistor	R_d	$0.02\ \Sigma$
Attenuation Factor	K_a	0.2
Switching Frequency	f_{sw}	2kHz
Boost Converter Freq.	f_c	5kHz
System Voltage	V_{gabc}	433V RMS

A standard temperature of 25ºC and a constant irradiation of $800W/m^2$ are considered. An incremental conductance based MPPT algorithm is used to derive maximum power from the DC-DC Boost converter stage.
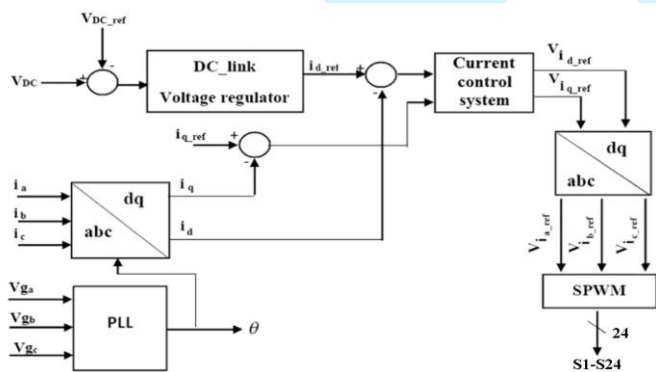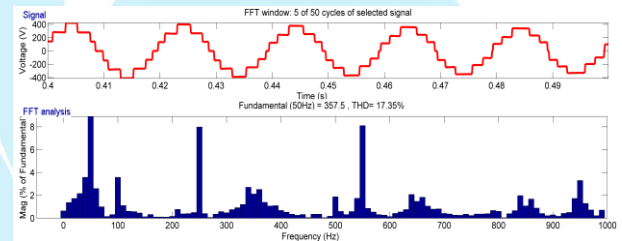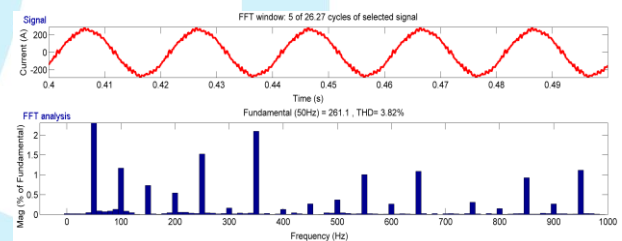

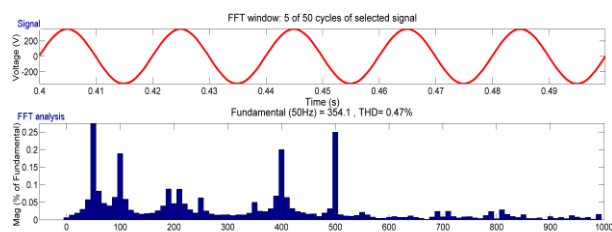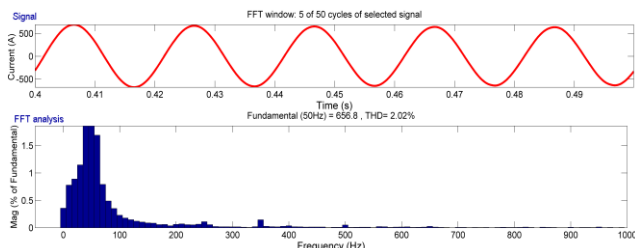Fig. 11.   Block Representation of Control System for Grid Tied VSI

Fig. 11 shows the schematic block diagram of the control system. The inverter is controlled by a current control strategy where dc link voltage is kept constant. A 22kV grid is connected to the point of common coupling using a step-down transformer of rating 315 kVA, 22kV/433V. Reference for d- axis current is provided by dc voltage in the outer control loop while the inner d-axis and q-axis current control loops regulated the injected current in the grid (i_q). As the system is considered to be balanced, zero sequence component of current is absent and only d-axis and q-axis currents are considered. SPWM pulses are derived using the reference voltages generated by inverse dq transformation.

The output line voltages and currents of the inverter are shown in Figs. 12 and 13 respectively. The I_{THD} and V_{THD} values without filter are 3.82% and 17.35% respectively.

Fig. 12. V_{THD} of Output Voltage without filter

Fig. 13. I_{THD} of Output Current without filter

After passing them through the low-pass LCL filter, high frequency switching components get reduced thereby lowering the THD values. The V_{THD} and I_{THD} values the grid connected inverter after filtering are 0.47% and 2.02% respectively and are shown in Figs. 14 and 15. It can be observed that the voltage and current waveforms are nearly sinusoidal with less harmonic distortion.

Fig. 14. V_{THD} of Output Voltage using LCL filter

Fig. 15. I_{THD} of Output Current using LCL filter

The THD values of currents and voltages of two, three and five level inverters are shown in Table III. It is seen that five-level inverter with LCL filter has least THD values and is best suited for Solar PV grid tied applications.

TABLE III
THD COMPARISON

Parameter	Two Level	Three Level	Five Level
Current before filtering	15.09%	7.71%	3.82%
Current after filtering	9.78%	4.47%	2.02%
Voltage before filtering	94.6%	40.58%	17.35%
Voltage after filtering	10.06%	4.57%	0.47%

V. CONCLUSION

This paper has presented a simulation study of a three phase five level diode clamped Solar PV grid tied inverter using a Phase Dissipation based SPWM strategy to control the inverter. A LCL filter configuration is used with grid tied inverter to reduce switching harmonics from entering the system and improve the power quality. Design basics of LCL filter are also indicated. A comparative analysis of two, three and five level inverters show that THD of the proposed inverter is lowest.

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