Serial Rapid IO high speed optical interface protocol for Indigenous MRI

Mahadev Dipnaik[1], Viren Ukey[2], Dhananjay Patel [3], Ranjana Gite[4], Dr. Sanjay Thakur[5]

[1,3,4,5] Department of Electronics and Telecommunication Engineering, Vidyalankar Institute of Technology, Mumbai, India [2]Society for applied Microwave Electronics Engineering and Research , Mumbai, India

[1]mahadev.dipnaik@vit.edu.in [2]viren@sameer.gov.in [3]dhananjay.patel@vit.edu.in [4]ranjana.gite@vit.edu.in [5] sanjaysingh.thakur@vit.edu.in

Abstract— **This paper presents the available literature on high speed Serial Rapid Input Output communication protocol. The MRI gradient amplifier system consists of a cabinet with a power supply and three Gradient Amplifiers. It is a three axes Gradient Amplifier system, which can be used in a MRI system to control the X, Y and Z Gradient Coils. The optical interface this current setpoint can be transmitted digitally to the Gradient Amplifier. The gradient amplifier system possess optical interface which is a high speed interface intended for communication of current setpints, system clock, control diagnostics by the MRI system host. This optical interface benefits from digital optical isolation and removes cable, conversion loses and noise on the current setpoint.**

Keywords- MRI system, Gradient amplifier, Serial Rapid Input Output, Optical interface.

1. Introduction

The Magnetic Resonance Imaging is an invasive technique used to form high resolution images for internal body tissues with no harmful radiation exposure. To determine the signal is coming from which part of the body we used Gradient coils which is nothing but a set of wires in the magnet, which create additional magnetic fields which superimposed on the main magnetic field B0. The gradient amplifier has three gradient coils. The Gz gradient selected an axial slice. The Gy gradient is used to determine phase encoding. The Gx gradient is used to determine frequency encoding.

In 1972, Paul Lauterbur established a new technique named as “NMR zeugmatography” which utilizes small linear magnetic field over the continuous uniform magnetic field to obtain encoding of spatial position into the frequency of the NMR signal [1].The technique proposed by Lauterbur remains the central idea for image formation in MRI. This requires an addition of three linear magnetic fields (Gx, Gy, Gz) along with main magnetic field around patient thereby varying resonant frequency with both spatial position and time. This method is being utilized to form images since the beginning of MRI development and prove to very successful and efficient [2]. Magnetic Resonance technique offers superior non-invasive imaging technique for visualization of soft tissue with no harmful radiation exposure [3].MRI remains the choice for Imaging Brain tumor imaging due to its excellent soft tissue contrast as compare to Computed Tomography Imaging [4]. MRI based electrical tomography technique has been adopted in detecting electrical conductivity and permittivity of human tissues by measuring variation in radio frequency of magnetic field in MRI. This technique allows measurement of specific absorption rate and detection of Cancer [5]. Recent development reveals three-dimensional imaging of internal anatomy and physiology of patients help in identification of diseases effectively and locating defects precisely without used of Ionizing agents which may have side effects on Patient in some cases [6].

The implementation of Gradient waveform synthesizer on Field programmable gate array employing linear algebraic equation. The algebraic equation is optimised to allocate minimum resource utilization on FPGA with highly efficient multipliers, Dividers, and Digital Signal Processor cores. Addition of DSP’s allows faster processing time and precise waveform generation with TCP/IP protocol. [7] .This Paper target the Gradient Amplifier optical interface is a high speed optic interface intended for communication of current setpoints, system clock, control and diagnostics by the MRI system host. The main features of this protocol is Galvanic isolation which eliminates interface noise ,Serial Rapid IO protocol , System clock synchronization , Digital current setpoint distribution and system monitoring.

This paper is structure as follows. In Section A , Gradient amplifier optical interface system with detail showing only main connections. Section B shows the literature on Serial Rapid IO protocol and SFP . Section C deals with Current Setpoint distribution using optical interface with two case examples without pre buffering and with prebuffering and also shows the Bandwidth calculation for MCE and current setpoint transaction The conclusion is presented in Section D.

A. Gradient amplifier Optical Interface system:

The Figure 1. shows the optical interface system with a functional level of detail showing only main connections. [10]

The optical interface protocol is Serial Rapid IO (SRIO), which is the main interface for accessing the Gradient Amplifier. Through SRIO two register interfaces can be accessed, High Speed register interface, direct interface for low latency and high bandwidth performance, accessing current setpoint distribution related registers . The internal register interface, distributed interface to all units registers within the Gradient Amplifier. Each register interface has its own transaction processor, which handles a read or write to its own registers. These interface processors separate transactions, so a read to the internal registers map which can have a slow response time, will not block the transactions on the High Speed register interface. This transaction processor can process one transaction at a time. Therefore a transaction request to one register interface must be completed before sending the next request to the same interface. When a second transaction is requested to the same register interface without completing the first transaction it will stall both register interfaces until it is completed.

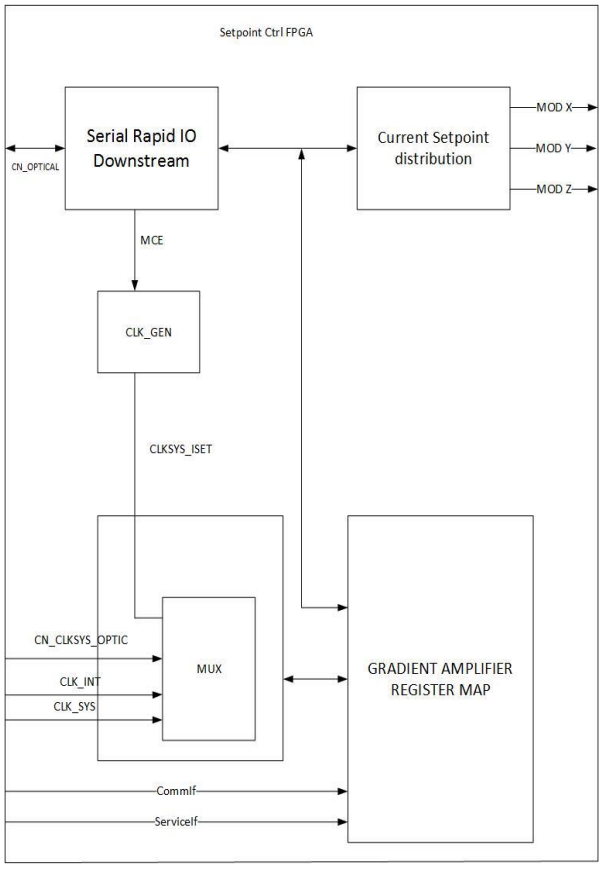

Figure 1.Gradient amplifier Optical Interface

Doorbells send by the Gradient amplifier are used for system error and warning notifications. The doorbell info field indicates an error or warning with the following code Error: 0x0E00,Warning: 0x0D00. When the Gradient amplifier is in error state or has a warning, a notification doorbell is sent to an endpoint device with target ID which can be configured in the Target ID register when the host receives a doorbell it can investigate the cause of the doorbell by reading the registers. The CLKSYS_ISET is added to the Gradient amplifier and can be selected by the Clk Sync mux for system clock synchronization through the optical interface. This clock is generated by the ClkGen using the optical interface Multicast-Event (MCE) symbols. The Clk Gen generates a 100kHz PLL based clock and locks this clock to the inbound MCE symbols. The MCE symbol is a standard Serial Rapid IO symbol for synchronizing systems, this symbol is used for generating the system (100kHz) clock. For this functionality the MRI host system must send MCE symbols at 100kHz.

B. *Serial Rapid IO Communication protocol:*

The optical interface protocol is Serial Rapid IO (SRIO), which is the main interface for accessing the Gradient Amplifier.The RapidIO has Up to 10 Gb/s of bandwidth, low latency and low power which increases the performance of rapid developing communication technologies. This protocol comprise a highly flexible and optimized Physical, logical and transport layer [8]. It has 1 lane 2.5GBaud ,Supports 34-bit addressing, Compliant to RapidIO specification ,Default SRIO 8bit base device ID: 0xA0 , AssyIdentity: 0x1600 , AssyVendorIdentity: 0x00A4, Recommended point-to-point connection, no influence from other traffic.It also supports Inbound SWRITE transaction ,Inbound NWRITE transaction ,Inbound NREAD transaction request ,Outbound NREAD transaction response, Outbound DOORBELL transaction, 32-bit aligned transactions only ,Maintenance transactions, Multicast-Event symbol, Little-endian Optical interface provides access to the gradient amplifier by the MRI host via an SFP compatible optical module. The link is intended for Digital current setpoint communication, system clock distribution. Software control communication. This interface also used for sending digital current setpoints to MOD X, Y and Z. Settings, status feedback and monitoring Distribution of system clock o Error read out and diagnostics ,Enable/Disable current generation. The SFP+ module is a hot pluggable small footprint serial-to-serial data-agnostic optical transceiver. The SFP8431 module is used to implement single-mode or multimode serial optical interfaces at 850 nm, 1310 nm, or 1550 nm.[11]

The Zynq FPGA processor is used rather than Microblaze processor because is used to performs more

computations with less energy and it directly reads from cache of CPU either goes from DRAM. The AXI interconnect is used to communicate with various IP modules.[9] The AXI master initiates the transaction and AXI slave respond the initiated transaction. GTH/GTY Transceiver is used to send the data to gradient amplifier through SFP8431 which is compactable with gradient amplifier SRIO protocol .The SFP is used to take the electrical signals and sends the optical signals through Transceiver. The figure2. shows the simulation results of SRIO with the third party software.

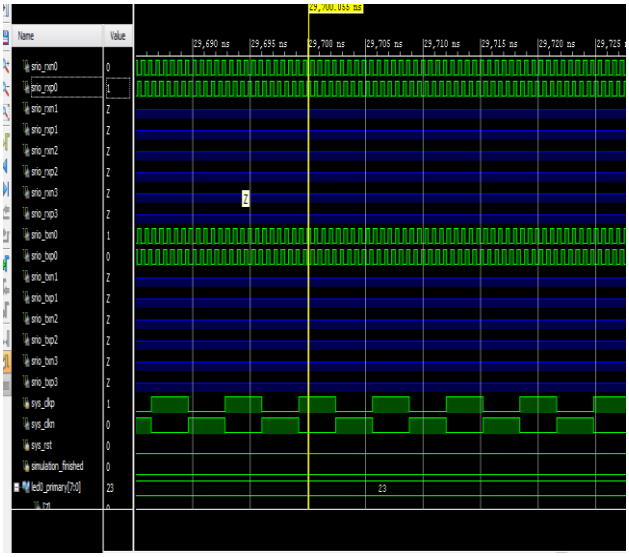

Figure 2. SRIO simulation with VIVADO software

C. *Current Setpoint distribution using optical interface:*

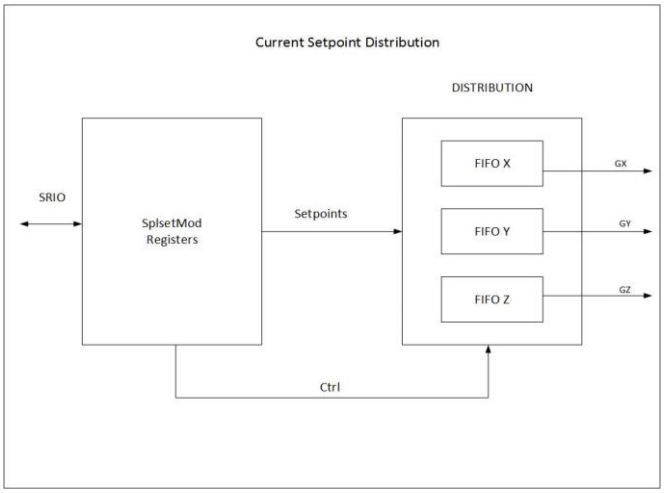

Figure3. Current setpoint Distribution

Current setpoints written to the SpIsetMod[X,Y,Z] registers are buffered in FIFO[X,Y,Z]. Each FIFO can hold up to 512 current setpoint samples, which can be used for pre-buffering samples and bursting samples into the FIFO. For bursting current setpoint samples, the SpIsetMod registers are incremental mapped so one SRIO packet can contain multiple current setpoints. The current setpoint samples in the FIFOs will be distributed through the system by setting SpIsetCtrl.DistrEnable. The rate of distributing the samples can be configured in the SpIsetCtrl.SamplePeriod register. When distribution is enabled the distribution and SamplePeriod clock starts on the first following CLKSYS_ISET (MCE symbol). In case of a FIFO underflow an error is set. It is up to the MRI host to assure that the FIFOs always contains sample(s) for each sample period. In case of communication jitter or SRIO retries it is possible that the FIFOs underflows, therefore it is recommended to pre-buffer current setpoint samples before enabling the distribution.Suppose we take two case examples without pre buffering means setpoints are send without using the FIFO, and with pre buffering means setpoints are send using burst and FIFO buffering functionality. The global parameters for gradient amplifier is configured to synchronize on CLKSYS_ISET (MCE), set in NgCtrl.ClkMuxSel. CLKSYS_ISET is already locked to the inbound MCE symbols send by the MRI host. Gradient amplifier is configured to digital current setpoint mode, set in CgCtrl. gradient amplifier is set to operational/enabled state. Sample Period is configured to 625kHz for optimized performance for gradient amplifier, set in SpIsetCtrl.SamplePeriod. Point-to-point connection,no influence from other traffic (low latency and jitter).

Without pre-buffering

System clock CLKSYS_ISET generated by ClkGen is locked to the inbound MCE symbols. Current setpoints sample ‘A’ is written to the FIFO and ‘e’ is set to enable distribution. Distribution is enabled and starts the SamplePeriod and distribution on the next CLKSYS_ISET (MCE symbol).

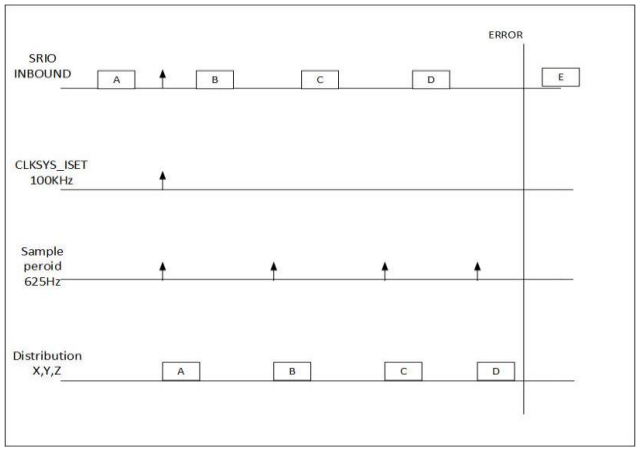

Figure 4. Current Setpoint Distribution (without pre-buffering) timing diagram

To assure that the distribution is enabled on the next MCE symbol, write the transaction with ‘e’ with enough margin

(2us) to the next MCE symbol. Current setpoint 'A' (X, Y and Z) is distributed on the Sample Period clock. Jitter (j) on the digital interface causes jitter on inbound transaction 'C', but because these are distributed on the Sample Period this jitter is removed. In this case it is important that the write transaction of the current setpoints must be scheduled with enough margin before the next Sample Period. Due to a communication error, transaction 'E' is retried and delayed. Transaction 'E' is delayed after the next Sample Period, causing an underflow on the distribution FIFO and sets the SetpointCtrl unit in error state.

Total SRIO Bandwidth :

Effective SRIO bandwidth

Total Bandwidth =2.5 Gbps*8b/10b= 2Gbps

MCE Bandwidth = 64 symbol packet*100Khz =6.4 Mbps

Required bandwidth from total bandwidth for MCE is 0.32%

Current setpoint NWRITE bandwidth:

Datapayload =32 b register*registers

Currentsetpointbandwidth=(packetoverload+datapayload)*sampleperiod=(160b+32b*4)*625khz=180Mbps

Required bandwidth from total bandwidth for current setpoint is 9%.

With pre-buffering

In this example, setpoints are send using burst and FIFO buffering functionality. This creates more robustness on the current setpoint distribution and uses SRIO bandwidth more efficient.

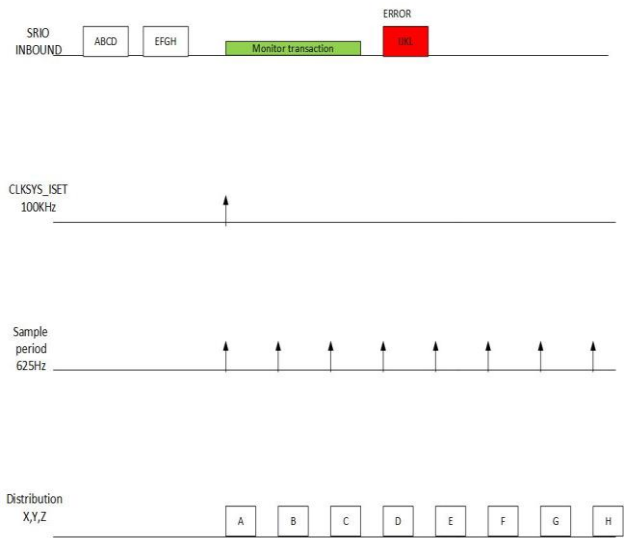

Figure 5. Current Setpoint Distribution (with pre-buffering) timing diagram

System clock CLKSYS_ISET generated by ClkGen is locked to the inbound MCE symbols. Current setpoints samples 'A,B,C,D' are written to the FIFO. Distribution is enabled and starts the SamplePeriod and distribution on the next CLKSYS_ISET (MCE symbol). To assure that the distribution is enabled on the next MCE symbol, write the transaction with 'e' with enough margin (2us) to the next MCE symbol. Current setpoint 'A' (X, Y and Z) is distributed on the Sample Period clock. The FIFO contains samples 'B,C,D,E,F,G,H'. Due to a communication error, Transaction 'I,J,K,L' is retried and delayed. Transaction 'I,J,K,L' is delayed after the next Sample Period, but does not cause an underflow on the distribution FIFO. Current setpoint 'E' (X, Y and Z) is distributed and the FIFO contains samples 'F,G,H,', due to pre-buffering. In this case a communication retry does not cause a system error.

Current setpoint NWRITE bandwidth:

Maximum Packet Size

Data payload=32bregister*registers*samples

Currentsetpointbandwidth=(packetoverload+datapayload)*sampleperiod/samples=(160b+32b*3*4)*(625Khz/4)=85Mbps.Required bandwidth from total bandwidth for current setpoint is 4.25%.

Conclusion

This Paper Gradient Amplifier optical interface is a high speed optic interface intended for communication of current setpoints, system clock, control and diagnostics by the MRI system host. By using SRIO protocols the digital current setpoint distribution which also reduce conversion loses and noise on the current setpoint . The effective use of SRIO bandwidth with or without pre-buffering is achieved using bandwidth calculation for MCE and current setpoint transaction .The Zynq processor is used for communication between console PC and gradient module which has inbuilt SRIO functionality.

References

[1] O. P. Simonetti, J. L. Duerk and V. Chankong, An optimal design methodfor magnetic resonance imaging gradient waveforms, IEEE Transactionson Medical Imaging, vol. 12, no. 2, pp. 350-360, Jun 1993.

[2] Sharp, J. C. and King, S. B. (2010), MRI using radiofrequency magnetic field phase gradients. Magn. Reson. Med., pp. 151-161, Nov. 2009.

[3] S. Nazarian et al., Feasibility of real-time magnetic resonance imaging for catheter guidance in electrophysiology studies, Circulation, vol. 118,no. 3, pp. 223-229, July 2008.

[4] Y. Kim, S. S. Cheng, M. Diakite, R. P. Gullapalli, J. M. Simard, J. P. Desai, Toward the Development of a Flexible Mesoscale MRI-CompatibleNeurosurgical Continuum Robot, IEEE Transactions on Robotics , vol.PP, no.99, pp.1-12, July 2017.

[5] R. Hong, S. Li, J. Zhang, Y. Zhang, N. Liu, Z. Yu, Q. H. Liu, 3-D MRI-Based Electrical Properties Tomography

Using the VolumeIntegral Equation Method, IEEE Transactions on Microwave Theory and Techniques , vol.PP, no.99, pp.1-10, July 2017.
[6] SPD: Product Specification Document of GRADIENT AMPLIFIER 1.3(Prodrive Technologies) R07,2015-06-05. SPD6001175449R03.pdf
[7]Implementation of MRI Gradient Generation System and Controller on Field Programmable Gate Array(FPGA), International Conference on Communication, Information Computing Technology (ICCICT), 2018.
[8] J. Adams, C. Katsinis, W. Rosen, D. Hecht, V. Adams, et aI., "Simulation experiments of a high-performance RapidIO-based processing architecture," Network Computing and Applications, Cambridge, USA, pp. 336-339, October 2001.
[9]UG585 ,Zynq 7000 SoC Technical reference manual,Xilinx.
[10] Requirements specification of NG1800 and NG1800-XP Anton Driessen, Tom van der Kant, Michel Hagenaar, Joost van Straalen.
[11] SFP+ 10 Gb/s and Low Speed Electrical Interface (SFF-8431) MSA Rev 4.1 September 2013.