ASIC Design flow of Image Signal Processor

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***Abstract*— ASIC Design flow of Image Signal Processor is discussed in detail in this paper. ISP is built to deliver high quality videos and images. Architecture is developed as per the specification. The RTL code is written for digital blocks and verified with verification techniques. Synthesis generates netlist of the design. Backend layout plan is carried out and GDSII is generated.**

Keywords*— *ISP, Synthesis, floor plan, STA, GLS, GDSII

I. INTRODUCTION

The Application specific integrated circuit (ASIC) is a type of IC that is designed for one specific application unlike a CPU or microcontroller, which is built to be general-purpose.

An ASIC is like a power tool designed for one task — faster, smaller, and more efficient for that task.

ASIC is expensive to design and fabricate, so it only make sense if it is produced in large quantities.

II. IMAGE SIGNAL PROCESSOR (ISP)

Inside the phone's camera there is a tiny ASIC called an Image Signal Processor. Image Signal Processor in short called as ISP. It is a dedicated hardware block in System on Chip (SoC) that is used to process video and images captured by camera. This ASIC is designed to deliver high-quality images and 4K/8K video while keeping battery consumption low.

It handles: noise reduction, color correction, HDR merging, face/scene detection and even many more tasks.

Example: Qualcomm Snapdragon (e.g., 8 Gen 1+), MediaTek Dimensity and Samsung Exynos.

III. ASIC DESIGN FLOW

The ASIC design flow of ISP is shown in figure 1. It starts with collecting and listing specification followed by developing and finalizing architecture of design. Writing optimized RTL code for digital blocks of design.

The RTL code is verified to ensure it is bug free design. Synthesis is done after verification signoff. DFT is inserted at this stage to make design testable

A detailed layout plan is carried out to build the design on silicon material and finally GDSII is generated. GDSII is sent to foundry.

These steps are discussed in details in this paper.

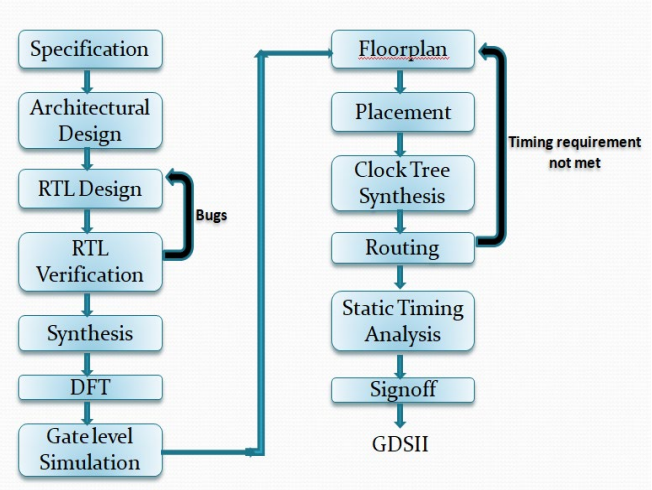

Fig. 1. ASIC design flow of Image Signal Processor

A. Specification

Defining the specifications of the design is first step in design process.

In this stage the detailed requirements for the chip are defined.

A good spec describes: functionality:

1. What the ASIC should do, performance throughput, clock speed, etc.
2. Interfaces Input/output standards
3. Power & Energy Max power budget, idle power., etc.
4. Area / Cost Target die size, manufacturing cost, and package type.

The inputs for specification is received from various teams sale, marketing, operation, design, etc.

For example the specification for ISP is given below:

a. Support sensors up to 200 MP

b. Video capture capacity: 8K@ 30 fps or 4K@ 120 fps

c. Triple camera concurrency: ISP supports to work with three lenses at once — wide, ultra wide, and telephoto — for smooth zoom, richer detail, and advanced imaging effects

d. Consume ≤ 600 mW at 4K/60 fps

e. Interfaces via MIPI CSI-2 (4 lanes):

MIPI CSI-2 = Mobile Industry Processor Interface – Camera Serial Interface v2.

It's the standard high-speed serial link used by cameras to send raw image data to an ISP.

B. Architectural Design

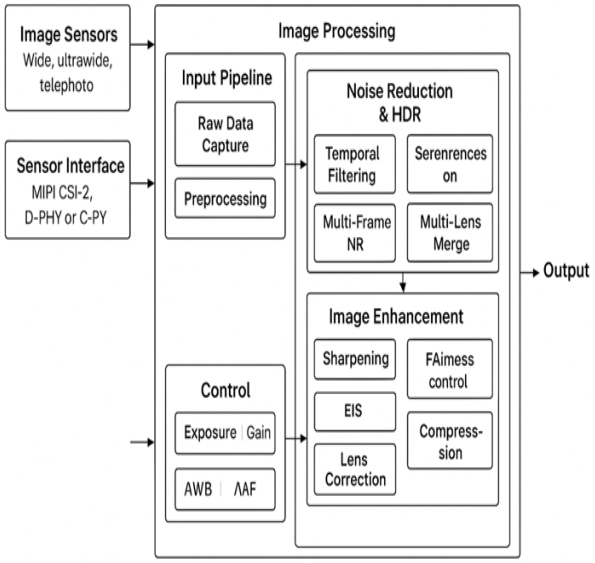

Fig. 2. ASIC design architecture of ISP

This involves determining the overall structure, the arrangement of functional blocks, and the interconnections between these blocks for ISp shown in fig 2..

Engineers must brainstorm many possible ideas. Engineers select the ideal approach by carefully considering the following things:

a. Performance implications.

b. Technical feasibility.

c. Hardware resources while keeping the overall cost within the assigned budget

d. Noise Reduction and HDR: This block make images clear, sharp, and balanced.

e. Image Enhancement: It is the stage where the goal is to make an image look better to the human eye without changing its basic content.

f. Control Block: The Control Block coordinates all other blocks.

C. RTL Design

In ASIC design Register Transfer Level (RTL) code is written for each digital block in the design architecture.

The high level language like Verilog/ VHDL/ System Verilog is used for coding.

The RTL design engineers focus only on functionality while writing the code using tools like Xilinx ISE, Vivado, etc.

RTL engineers write linear testbench to verify the functionality using simulator like Xilinx ISE, Model- Sim.

D. Verification

RTL verification ensures that an ASIC behaves as intended through simulations and other verification techniques.

RTL Verification ensures it is bug free design.

Verification engineer uses Hardware Verification Language (HVL) like system Verilog and Universal Verification Methodology (UVM)

Synthesis

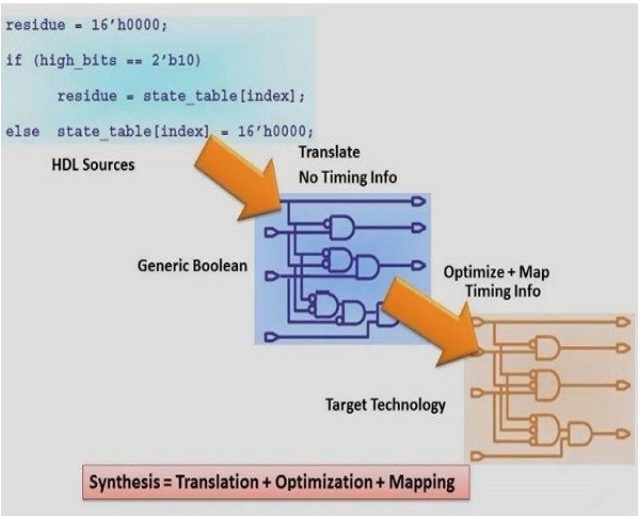

Fig. 3. Synthesis process

Synthesis is a process which converts RTL code into optimized gate level netlist shown in fig 3.

Synthesis is done using EDA tools like Cadence, Synopsys, Siemens, etc

EDA tool is called as Synthesizer.

Synthesis technique involves two major steps

a. Translation: RTL code is translated into Boolean gates.

b. Gate mapping: Boolean gates are mapped to target technology and optimized with respect to constraints.

E. Design for Testability (DFT)

DFT stands for design for testability where DFT engineers add extra hardware block as a part of design.

DFT make sure that chip is testable.

DFT components are added during this phase helps testing of chip once it is manufactured.

DFT guarantees fault free chips.

The test patterns are generated to test the defects that includes stuck at faults, IDDQ faults, delay faults.

Stuck at faults is due to connecting particular input or output pins of the circuit to VDD or ground.

IDDQ faults due to shorting of transistors and delay faults are slow to rise or slow to fall faults.

F. Gate Level Simulation (GLS)

Gate Level Simulation (GLS) is a crucial step in the ASIC design verification process, occurring after the synthesis of the Register Transfer Level (RTL) code.

It involves simulating the behavior of a circuit at the gate level, using a netlist.

Netlist represents the circuit in terms of logic gates and their interconnections.

Unlike RTL simulations, which typically operate in a zero-delay environment, GLS can incorporate timing delays. These delays can be specified using Standard Delay Format (SDF) files.

It allows for more accurate modeling of real-world behavior where propagation delays and signal integrity are critical.

GLS is crucial for verifying timing, power, and low-level design features like tri-state buses and clock gating.

G. Floorplan

Floor plan is the process of strategically arranging functional blocks, I/O pads, and power/ground structures on the chip as shown in fig 4.

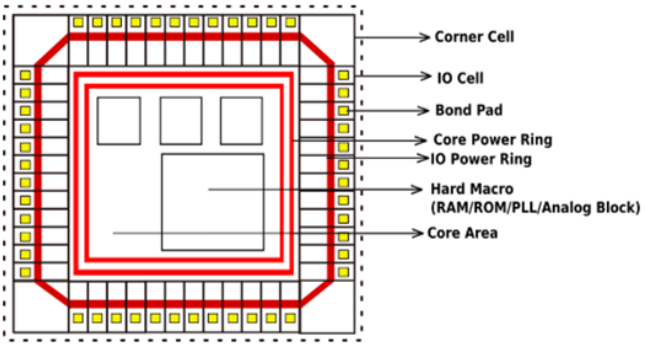

Fig. 4. Floo rplan

Netlist is one of the inputs for floor planning which describes logical description of the ASIC design.

It optimizes various factors like area efficiency, signal integrity, and power delivery.

It essentially defines the physical layout of the chip.

H. Placement

Placement involves arranging standard cells within a defined area to minimize wire length, optimize timing, and reduce congestion.

Before placement, a floor plan is created to define the overall layout of the chip, including the placement of major blocks and the allocation of space for different regions.

Placement also does optimization which involves refining the initial placement, often using algorithms to minimize wire length, optimize timing, and reduce congestion.

This process is crucial for meeting performance requirements and ensuring the chip's functionality.

H. Clock Tree Synthesis (CTS)

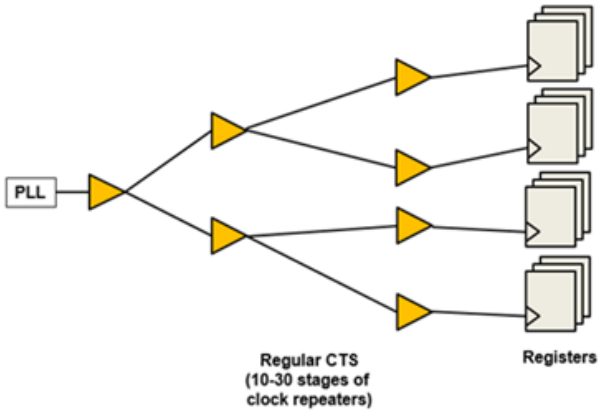

Fig. 5. Clock Tree Synthesiss

Clock Tree Synthesis structure is shown in fig 5.

CTS aims create a balanced clock distribution network where all clock sinks (flip flop) receive the signal at the same time.

CTS techniques ensure minimal skew (differences in arrival time).

I. Routing

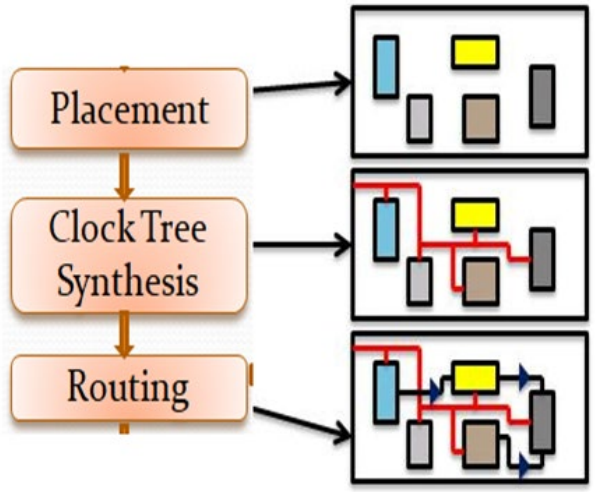

Fig. 6. Routings process

Routing process is shown in fig 6 in which physical design engineer routes interconnection and metallic contacts.

Routing is the physical design stage where interconnecting wires, or metal paths, are created to connect the cells and I/O pins based on the logical connectivity defined in the netlist.

Routing ensures that signals can flow between different parts of the chip.

It is a key factor in meeting performance requirements.

J. Static Timing Analysis

STA is a method used to determine if a design meets timing constraints.

It ensures that signals are propagated and synchronized correctly throughout the entire chip.

Static timing analysis aims to ensure that a given design, with the specified input clock definitions and the external environment parameters, can function at the intended speed without any timing issues.

The core of STA involves analyzing the circuit using the netlist, cell characterization, and timing constraints to calculate timing metrics.

Once STA is completed, detailed timing reports are generated, highlighting critical paths and potential setup/hold violations. Using the timing report, engineers can optimize the design iteratively.

K. Signoff

Signoff is the process of verifying the design at final stage before going to the tape out.

Clean signoff reports are the green signal.

Tape out refers to the final stage where the completed chip design, including all design, verification, and layout work, is sent to a semiconductor foundry for manufacturing.

Before tape out, the design is meticulously checked for manufacturability, including Design Rule Checks (DRCs) and Layout Versus Schematic (LVS) checks.

The term "tape out" historically refers to the physical transfer of design data, often on magnetic tape, to the foundry.

L. GDSII

GDSII stands for Graphic Data System II.

It is a binary file format used to represent the physical layout of integrated circuits.

This format is crucial in the chip design flow, as it provides the complete geometric details of the chip's layers, shapes, and interconnections.

IV. CONCLUSION

The ASIC Design flow of Image Sensor Process a tiny IC inside the Smartphone is discussed detail in this processor. The RTL design of architecture of ISP is carried out followed by verification and synthesis. Once netlist is generated, DFT components are inserted to ensure chip testable. The netlist is input for backend physical design process where floorpan, placement and static timing analysis is carried out. The final GDSII is generated after the tape out.

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