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High Resolution DPW Modulator based on FPGA with Linear behavior of system

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***Abstract*—Digital pulse width modulator (DPWM) have so many advantages in Power Electronics field. So there is increase in use of DPWM in various applications. There are so many DPWM designing techniques are available. Among these, the classical design techniques will require higher frequency clock signals. Also the linearity in the output is lost. This paper presents a design to increase the resolution of the DPWM with more linearity in the output which can be simulated and tested on field programmable gate arrays (FPGA). In some designs implemented FPGA have large code length. The proposed method is based on the on-chip digital clock manager block (DCM) present in the low-cost Spartan-3 FPGA series which helps to introduce new method of generating DPWM. Implementation of this will be very helpful considering various industrial applications.**

***Index Terms*—Field programmable gate arrays (FPGA), power conversion, power converters PWM.**

I. INTRODUCTION

Digital Pulse Width Modulation (DPWM) is crucial part of all embedded systems. It is widely accepted as control technique in most of the electronic appliances. From past few years these techniques were searched [1]. There are so many methods available depending on architecture and requirement of the system. This design implementation depends upon application type, power consumption, semiconductor devices, performance and cost criteria all determining the PWM method [1]. In digital control architecture Digital pulse-width modulators (DPWMs) plays a key role in any power converter [2]. DPWM can be implemented by making use of DSPs or FPGAs or custom hardware or custom hardware plus software. The DPWM frequency is mainly measured by the power converter operating conditions, where the DPWM resolution will determines the accuracy in the output. The DPWM resolution will directly effect on the power converter performance. Many traditional DPWM architectures are present which includes: counter comparator based architecture, Delay line architecture, Hybrid DPWM architecture, segmented delay line architecture, dithering, etc. [3]. Traditional DPWM based on counters and comparators generate the power converter control signals (gating s/g's) according to several predefined thresholds [4]. Now days, power converters are evolving toward designs with higher changing frequencies in order to reduce the size of circuits.

Several FPGA-based solutions have also been proposed in the literature [5], [6].One common solution is to use a coarse resolution counter-based stage plus one or several on-chip digital clock manager (DCM) blocks. The PWM signal is set at the beginning of the counter period, and it is reset after a given number of clock cycles plus a certain fraction of the clock period established by the DCM.

The aim of this technique is to provide a fully synchronous high-resolution DPWM architecture in order to avoid the need of using unfeasible high clock frequencies, providing a more convenient final implementation along with linearity in output. This technique is based on the resources available in modern FPGAs. The DCM based architecture allows operating the circuit at higher clock frequencies [7]. Higher switching frequency helps in enhancing the dynamic performance and hence provides higher DPWM resolution.

II. DCM BLOCK

The Spartan-3 devices provide control over clock frequency, phase shift and skew with the use of the DCM feature. To get this, the DCM employs a Delay-Locked Loop (DLL) that uses a feedback to maintain clock signal characteristics with a higher accuracy without any variations in operating temperature and voltage. Each member of the Spartan-3 family has four DCMs, except the smallest, the XC3S50, which has two DCMs. The DCMs are located at the ends of the outermost Block RAM column(s). The DCM will support three major functions [8]

1. Clock-skew Elimination: Clock skew describes the extent to which clock signals deviate from zero-phase alignment. When slight differences in path delays cause the clock signal to arrive at different points on the die at different times, clock skew takes place. It will increase set-up and hold time requirements as well as clock-to-output time, which is not suitable in applications operating at a high frequency.

The DCM eliminates clock skew by aligning the output clock signal it generates with another version of the clock signal that is fed back. As a result, the two clock signals have zero-phase shift. This effectively cancels out clock distribution delays that may lie in the signal path leading from the clock output of the DCM to its feedback input.

2. Frequency Synthesis**:** Provided with an input clock signal, the DCM can generate a wide range of different output clock frequencies. This is consummate by either multiplying and/or dividing the frequency of the input clock signal by various different factors.

3. Phase Shifting: The DCM provides the ability to shift the phase of all its output clock signals with respect to its input clock signal. The schematic of DCM block is shown in below Fig. 1

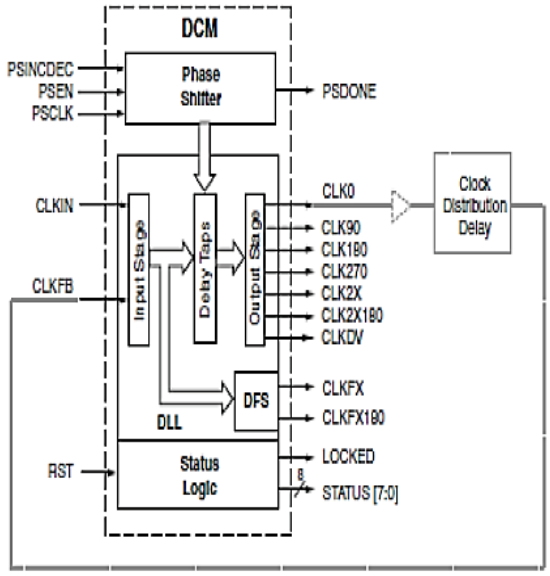

Fig. 1. DCM Functional blocks and associated Signals. [8].

III. HIGH RESOLUTION DPWM ARCHITECTURE USING DCM BLOCK

The key of this architecture is the on-chip DCM block provided in almost every state of the art FPGA. The following are the DCM clock management features [9].

1) Phase shifting: The DCM provides four phase-shifted clock signals derived from the source clock CLKIN. In addition to CLK0 for in-phase alignment to the CLKIN signal, the DCM also provides the CLK90, CLK180, and CLK270 outputs for 90◦, 180◦, and 270◦ phase-shifted signals, respectively. Besides, all the outputs of the DCM can be phase shifted with finer resolution.

2) Frequency synthesis: The DCM can generate a wide range of output clock frequencies (CLKFX output port), that will perform clock frequency division and multiplication. Besides phase shifting, the DCM is able to condition the clock input CLKIN in order to obtain clock outputs with 50% duty cycle. The clock feedback signal CLKFB is being used to compare and lock the output signals with the input CLKIN signal. The fine phase shifting can be fixed (specified at the time of design and set during the FPGA configuration process) or variable.

It is set by means of the DCM attribute PHASE_SHIFT, an integer in the range [−255, +255]. Below figure shows the fine phase shift effects in the fixed mode of operation. A phase-shifted output with a resolution of (1/256)th of the input clock period can be obtained. The variable phase-shifting feature has been used in [10]. However, this operating mode requires several clock cycles to change the duty cycle that will degrade the dynamic performance. Besides, an asynchronous circuit is used to divide the clock cycle into four quadrants as CLK0, CLK90, CLK180 and CLK270.

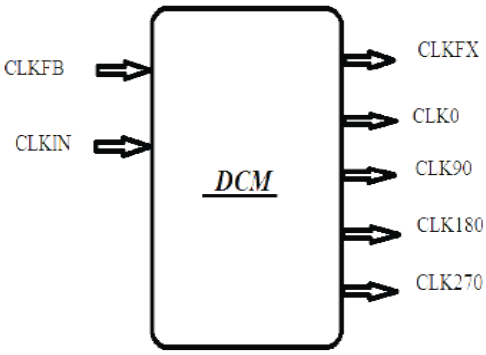

Fig. 2.Simplified pinout description of DCM block.

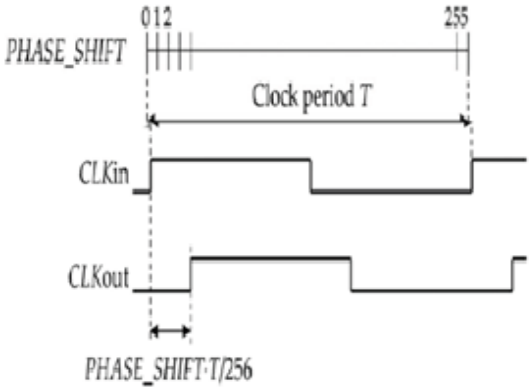

Fig. 3. Fixed fine phase shifting effect.

Detail Block Diagram of Proposed system

Below Fig. .4 shows the detailed block diagram of the proposed system. The first block in this system is DCM block which is present on almost all FPGA kit. It acts as an on-chip clock manager block. Spartan-3 devices provide flexible, complete control over clock frequency, phase shift and skew through the use of the DCM feature. To accomplish this, the DCM employs a Delay-Locked Loop (DLL), a fully digital control system that uses feedback to maintain clock signal characteristics with a high degree of precision notwithstanding normal variations in operating temperature and voltage. Various quadrant phase shifted output of DCM is given as input to multiphase circuit. The multiphase circuit makes use of D-ff and multiplexer circuit to generate RESET signal which is then given to SR-ff to generate a PWM output. The next block is PWM generator block which makes use of counter, comparator and D-ff to generate SETD, CLRD and SET signals. We can generate PWM output by making use of SET signal and RESET signal (which is output of multiphase circuit).

The generated PWM signals are then transmitted to a Drive circuit which then controls the external hardware. The hardware may consist of circuitry whose functioning is depends on PWM. The hardware circuitry may consists speed controlling of DC motor, Inverter or other power electronic devices which can controlled by PWM. By proper design of PWM we can consume very less power and it may help in power saving application.

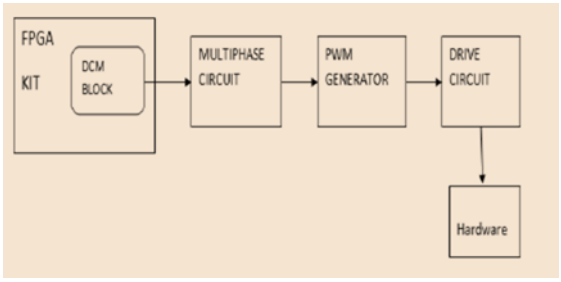

Fig. 4. System block diagram.

IV. DCM-BASED HRPWM APPROACH

In order to introduce the proposed DCM-based high resolution DPWM architectures with more linearity, the following architecture can be implemented, which is shown in below Fig. 5. In this the quadrant phase-shifted outputs of a single DCM are used.

The duty cycle command dc(m:0) has m+1 bits, ranging from m to 0, where m is most significant bit of duty cycle command, and the counter "CNT" has m−1 bits. "CLRD" signal is set when the m−1 most significant bits (MSBs), dc(m:2), are equal to CNT; and SETD signal is set when CNT is equal to zero and dc(m:2) is different from zero.

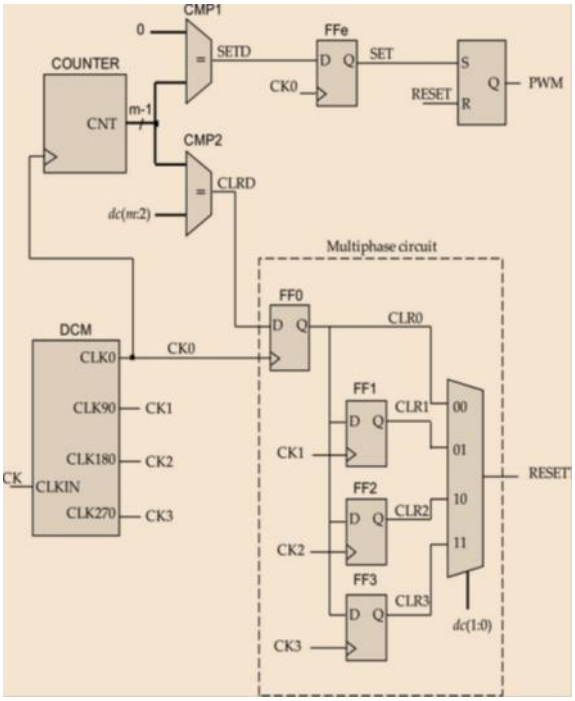

Fig. 5. DCM -based HRPWM first approach

Fig. 6. shows how the circuit works with m = 4, and dc = "10010". Basically, when the counter

CNT is equal to the m−1 MSBs of the duty command dc, signal CLRD activates. The resulting pulse is captured in the next clock cycle by FF0, and phase shifted 90˚, 180˚, and 270˚ by flip-flops FF1, FF2, and FF3, respectively. These four FFs implement a multiphase synchronous circuit [11]. The two least significant bits (LSBs) of the duty command are used by the multiplexer to select the phase-shifted signal that clears the SR latch. The advantage of this proposal in relation to others is that the digital circuit that generates the reset of the SR latch is synchronous. The use of asynchronous circuits to reset the latch makes harder to calculate timing using static timing analysis and can result in glitching since controlling the logic and routing delays in an FPGA is more difficult than in ASIC implementations. We can improve an above shown architecture in order to improve the HRPWM resolution. For the improvement of resolution of PWM certain relationship has to be maintaining between total numbers of different components of circuit. This relation is explained in below section.

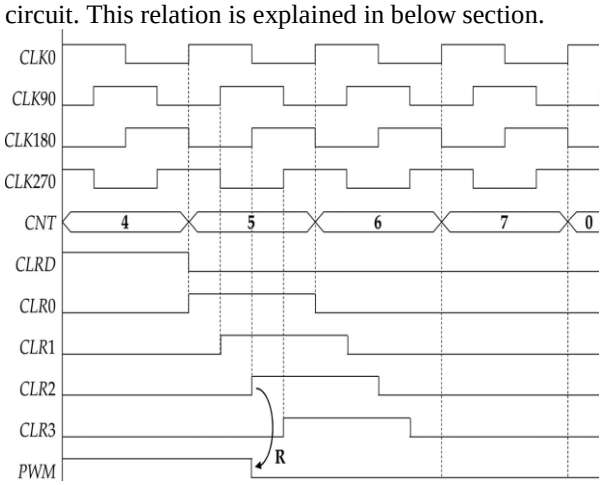

Fig. 6.DCM-based HRPWM operation with dc = "10010."

V. RESULT

The proposed system is implemented on Spartan 3E family of FPGA (XC developed by Xilinx. The testing of final results is done on Xilinx software. For the proposed system the PWM variation is totally based on value of "dc". The behavior of DCM block i.e. phase shifted outputs of DCM blocks (0^0 phase shifted, 90^0 phase shifted, 180^0 phase shifted and 270^0 phase shifted) are shown in below Fig. 7.

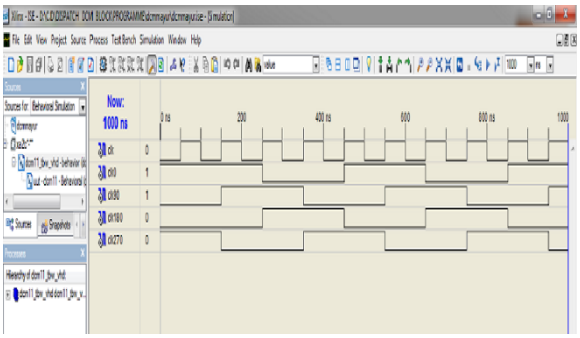

Fig. 7.Quadrant phase shifted output.

Below Fig. 8 to Fig. 11 shows some outputs according to variation of value of dc(12:0).

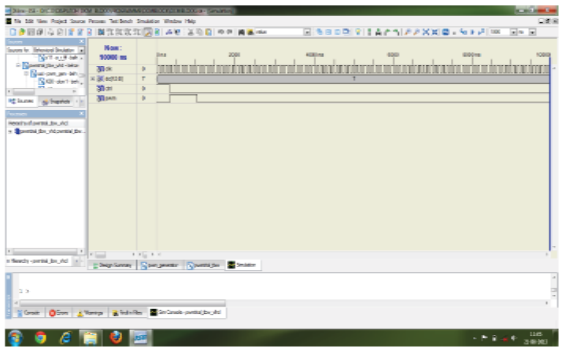

Fig. 8. PWM waveform for dc=0000000000011

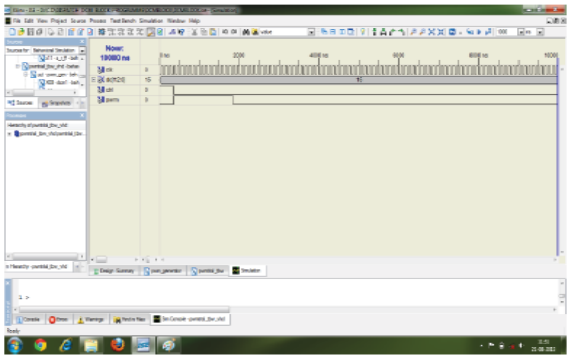

Fig. 9. PWM waveform for dc=0000000001011

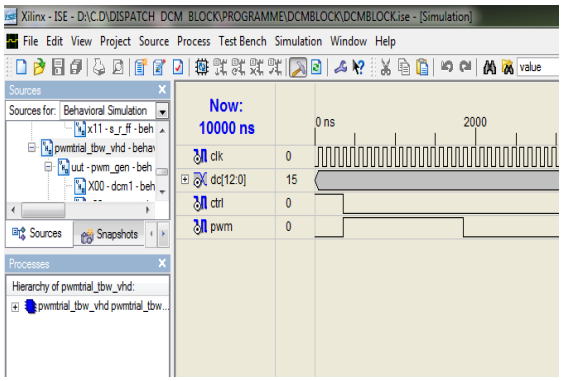

Fig. 10.PWM waveform for dc=0000000001111.

According to results shown above it can be seen that for each change in bit pattern there is change in ON time of output pulse. Here it is seen that ON time variation due to single bit change is of 100 ns.

The linear behavior of system can be shown by plotting graph of variation of DC command with respect to ON time of pulse (Ton). This graph is shown in Fig. 12.

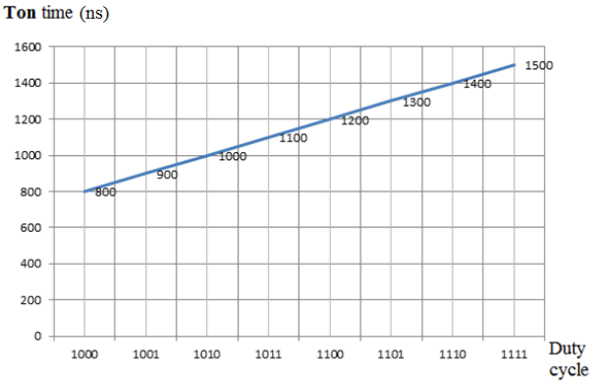

Fig. 11. DCM-based HRPWM architecture performance for duty cycle commands from "0000000001000" to "0000000001111".

VI. CONCLUSION

To make the development in power Electronics and Digital Electronics field, the development in resolution of DPWM along with linearity in output is necessary. These high resolution DPWM's are used in high frequency and high precision power convertors. In this paper, we have proposed a fully synchronous HRPWM implementations using different FPGA resource i.e. the DCM block. The DCM-based architecture is implemented using the resources present in low-cost FPGAs, and the maximum clock frequency is determined by the DCMs. These solutions are complementary and cover a wide spectrum of cost/performance applications. The proposed DCM-based synchronous architectures have been implemented on a Xilinx Spartan-3E.

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